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Design of Power Supply Unit for Passive UHF RFID Tag

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Abstract: *The survey and development of power supply unit for passive RFID tag functioning on ultra-high frequency are presented in this paper. RFID (radio-frequency identification) is a technique of objects identification in which data, stored in radiofrequency transponders or tags, is read and wrote by means of radio signals. One of the most important parts of RFID tag providing the energy for proper operation of tag is power supply module. Power supply unit can include such cells for harvesting and provision of energy as voltage rectifiers and multipliers, voltage regulators, bias schemes and others. This work considers design features of the rectifier with voltage multiplying which is capable to provide rectified voltage of 1.2 V while input radiofrequency voltage amplitude is less than 0.7 V. The circuit functions at 2.45 GHz frequency and is designed for implementation using 90 nm CMOS technology. Comprehensive simulation of the rectifier operation with variations of determining parameters was conducted. Besides, the voltage reference for voltage regulator was also developed and simulated.*

Keywords: *UHF RFID tag, power supply unit, voltage rectifer, multistage circuit, CMOS technology*

1. INTRODUCTION

Radio-frequency identification devices are used primarily for automatic identification and tracking of different objects in logistics and production chains. Moreover they have found practical use in toll collection, access control systems and cashless payment operations. Generally RFID system consists of transponder, reader and server with databases to which the reader addresses when it requests and process received information. Data and energy are usually transferred between tag and reader through microwave radiation (backscattering) or inductive coupling [1]. Radio-frequency identification tags usually include analog high-frequency cascades, modulation and demodulation units, digital processing schemes and, in some cases, memory elements, Figure 1 [2]. In addition auxiliary schemes of different purposes, like clock oscillator or mode selector, can be incorporated in a tag. In process of RFID tags design the problems related with matching between microchip and tag's antenna should be resolved in order to obtain acceptable performance and required reading distance.

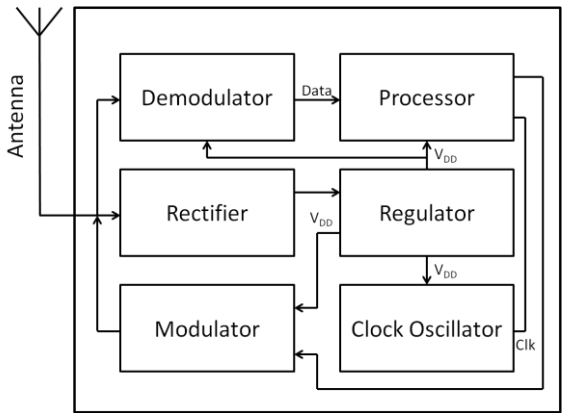

Figure1. *Block diagram of passive UHF RFID tag [2]*

Functional units responsible for conversion the energy of HF signal to DC voltage play a key role in operation of the transponder. Due to usage of various modifications of voltage rectifiers, regulators and limiters, microcircuit of the passive tag can have enough power both for correct functioning and for transmission the backscattering signal. In this paper we described the design of multistage half-wave voltage rectifier circuit intended for operation in a passive UHF RFID tag as well as the structure of voltage reference which is able to produce the input voltage for voltage regulator.

2. PROPOSED POWER SUPPLY MODULE FOR PASSIVE RFID TAG

2.1. TECHNOLOGICAL ASPECTS OF THE DESIGN

Design of power supply of passive RFID tag has been carried out for assumed implementation in CMOS technological process with 90 nm design rules and threshold voltage of NMOS V_{th} = 0.28 V. Employment of strained silicon to speed up carrier mobility in the channel of transistor became one of the most important innovation related with 90 nm technology. Horizontal strain can be created by the silicon nitride capping layer [3] or mixed semiconductor silicon-germanium (SiGe) [4]. The strain increases the distance between atoms under the gate. Since dispersal of atoms leads to advance of carrier mobility, saturation current increases by 10 – 25% [4].

During the design of power supply of passive RFID tag, transistors with low-leakage current have been used. These transistors are described by BSIM4 model. Besides, the type of high-speed transistor was reviewed. These types of MOS devices differ from each other mainly in values of threshold voltage (V_{th} = 0.26 V for high-speed transistor) and channel-length offset parameter LINT. LINT is equal to 0.015 μm for low-leakage transistor and 0.019 μm for high-speed one. High-speed MOS is characterized by higher values of forward current I_{ds} (740 μA at a voltage 1 V while for low-leakage NMOS transistor I_{ds} = 630 μA at similar voltage). Hence resulting voltage at the output of rectifying circuit slightly increases.

However reverse currents also increase approximately one and a half orders of magnitude in such transistor. In the case of low-leakage transistor reverse current is about 30 nA (at voltages V_{bs} = 0 and V_{gs} = 0) and in the case of high-speed transistor – about 300 nA. Since PCE (power conversion efficiency) of rectifying circuit decreases when leakage currents grows [5] and this efficiency is not high enough in charge pump schemes compared to bridge rectifiers, it is necessary to maintain reverse current at the lowest possible level. And use of low-leakage MOS transistor facilitate to this.

2.2. Design of Power Supply Module

Voltage rectifier circuit plays a major role in powering the units of radiofrequency tag by DC voltage. So far as bridge rectifier circuits can show insufficient values of supply voltage at ultra-high frequency [6], half-wave rectifier with voltage multiplying also known as Dickson's pump circuit was taken as a basis [7]. The diodes had been used in traditional circuit for conversion alternating current to direct current since the current flows in one direction in these devices. However voltage drop on silicon diodes is usually 0.6 - 0.7 V, therefore either voltage at circuit input should be high enough to attain satisfactory results or rectifying voltage will be small. Currently diode-connected MOS transistors are often used in rectifying circuits instead diodes. To form the diode-connected transistor its drain is coupled with its gate. Since in this instance turn-on voltage of transistor is approximately equal to its threshold voltage (V_{th}) [8, 9], this parameter should be reduced to a minimum. Also known cases of using Schottky-barrier diodes as rectifying cells which can operate at even less turn-on voltages but fabrication these circuits requires additional technological operations like photolithography so manufacturing cost increases.

According to the analysis, designs of passive RFID tags are more often focused at frequency band 860 – 960 MHz while for operation at frequency 2.45 GHz designs of active tags are mostly presented. For this reason design of the rectifier circuit of passive tag functioning at 2.45 GHz was in particular interest. Furthermore, this frequency has a number of advantages: absence of necessity for licensing, possibility of using inexpensive flexible antennas in transceivers, satisfactory reflection from metal surfaces, adoptable penetration through non-conducting mediums [1].

Capacitors are used in rectifier circuits for charge pumping and charge accumulation. As can be seen from Figure 2, couple of capacitors is usually included in the single stage of rectifier with voltage multiplying. Capacitor C1 is charging through diode D1 during a negative half-wave of sinusoidal

signal with amplitude V_{RF}. Diode voltage is equal to $V_{RF} - V_D$, where V_D – turn-on voltage of the diode. During subsequent positive half-wave capacitor C2 is charging through diode D2. The charge accumulated in capacitor C1 is transferred to this capacitor too. So output voltage can be estimated in the following way [8]:

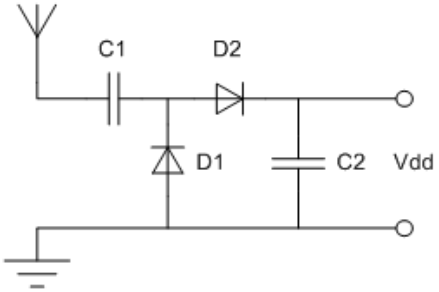

Figure2. *Voltage doubler circuit [8]*

$$V_{DD} = V_{RF} + (V_{RF} - V_D) - V_D = 2(V_{RF} - V_D). \quad (1)$$

Diode-connected MOS transistors are employed in proposed design instead of diodes but functioning principle remains the same. In the limit, when voltage V_D can be neglected, the circuit doubles voltage thereby it was so termed. With increase the number of stages at small voltage drops the output voltage can be expressed as

$$V_{DD} = 2N(V_{RF} - V_D), \quad (2)$$

Where N – number of stages in circuit.

Actually, the output voltage attains lower values because of different energy losses. It will not succeed to add stages indefinitely since the more stages in the circuit the more energy is lost at the rectifying cells resulting in diminishing return effect.

One can preliminarily estimate the values of the capacitances used in the circuit from the value of the time constant t. If this time required for capacitor discharge is long enough compared to high-frequency cycle time, supply voltage will be approximately permanent during this cycle. The time constant can be expressed as

$$t = RC, \quad (3)$$

Where C – capacitance, R – load resistance of the circuit.

In the proposed design the load resistance is substituted by equivalent resistance. This parameter can be estimated either by direct review of similar rectifier circuits [10, 11] in which load is 100 – 200 kΩ or by using expression for power consumed by the circuit:

$$P = \frac{V^2}{R} \rightarrow R = \frac{V^2}{P}, \quad (4)$$

Where V – supply voltage.

It is known from literature analysis [8, 10, 12] that average power consumed by UHF tag is usually from several units to several tens μW. Assuming P is equal to 10 μW and considering required supply voltage as 1.2 V, total load resistance of the tag is obtained equal to 144 kΩ. The obtained value R is consistent with the values of load from analyzed developments, therefore, the load value is taken as 100 – 200 kΩ in the design of power supply unit. Considering that the duration of high-frequency cycle (period of oscillation) for signal at frequency 2.45 GHz is T = 0.4 ns and time constant should be at least ten times more than period ($t > 10\ T$) [8], from (4) the order of magnitude for capacitances in multiplier circuit is equal to 40 fF. During testing the various options of the designed circuit, capacitances have been selected with allowance for obtained estimated value.

To attain acceptable values of supply voltage in proposed design NMOS devices with enlarged channel width W have been used. It is known from literature analysis that ratio W/L for transistors in rectifier circuits varies from 8 [13] to 85 [12] and more. Large ratio W/L leads to both high saturation

current and substantial reverse currents. Hence the output voltage increases but power efficiency decreases. So different options of ratio W/L have been reviewed in the process of design and acceptable value 20 was chosen.

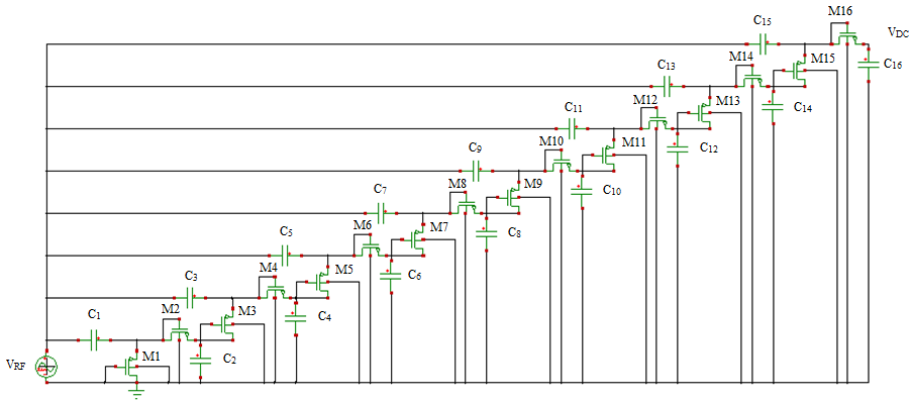

Figure3. *Schematic circuit of proposed voltage rectifier*

The schematic circuit of designed 8-stage rectifier with voltage multiplying is shown in Figure 3. DC voltage obtained at the circuit output reaches 1.22 V at input signal amplitude of 0.7 V and frequency of 2.45 GHz. Figure 4 shows the layout of 8-stage rectifier. The area of each odd capacitor (C = 200 fF) is equal to 960 μm^2, the area of each even capacitor (C = 150 fF) is 720 μm^2. One transistor with enlarged channel width (W/L = 20) occupies the area 1.44 μm^2. The total area of rectifier is 0.0153 mm^2.

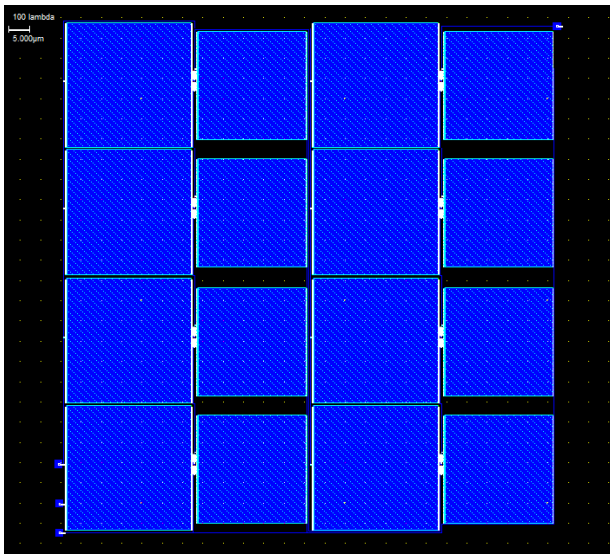

Figure4. *The layout of rectifier with capacitors performed in 4 metal layers*

Moreover during the design of power supply module for passive RFID tag, reference-voltage source for voltage regulator of the tag was developed. Structure of this functional unit was created based on constructions from [14]. In this instance reference-voltage consist of three NMOS and one PMOS diode-connected transistors as it shown in Figure 5.

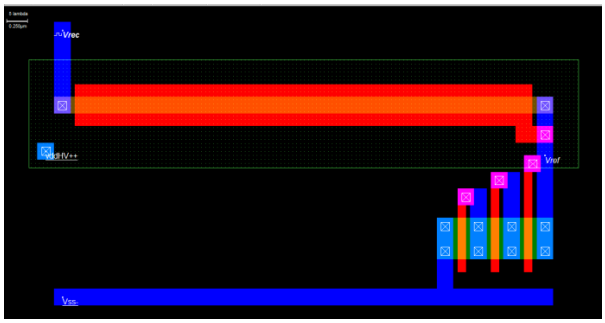

Figure5. *The layout of reference-voltage source*

3. Simulation and Discussion

The simulation of rectifying structure has been carried out in circuit simulation environment T-Spice.

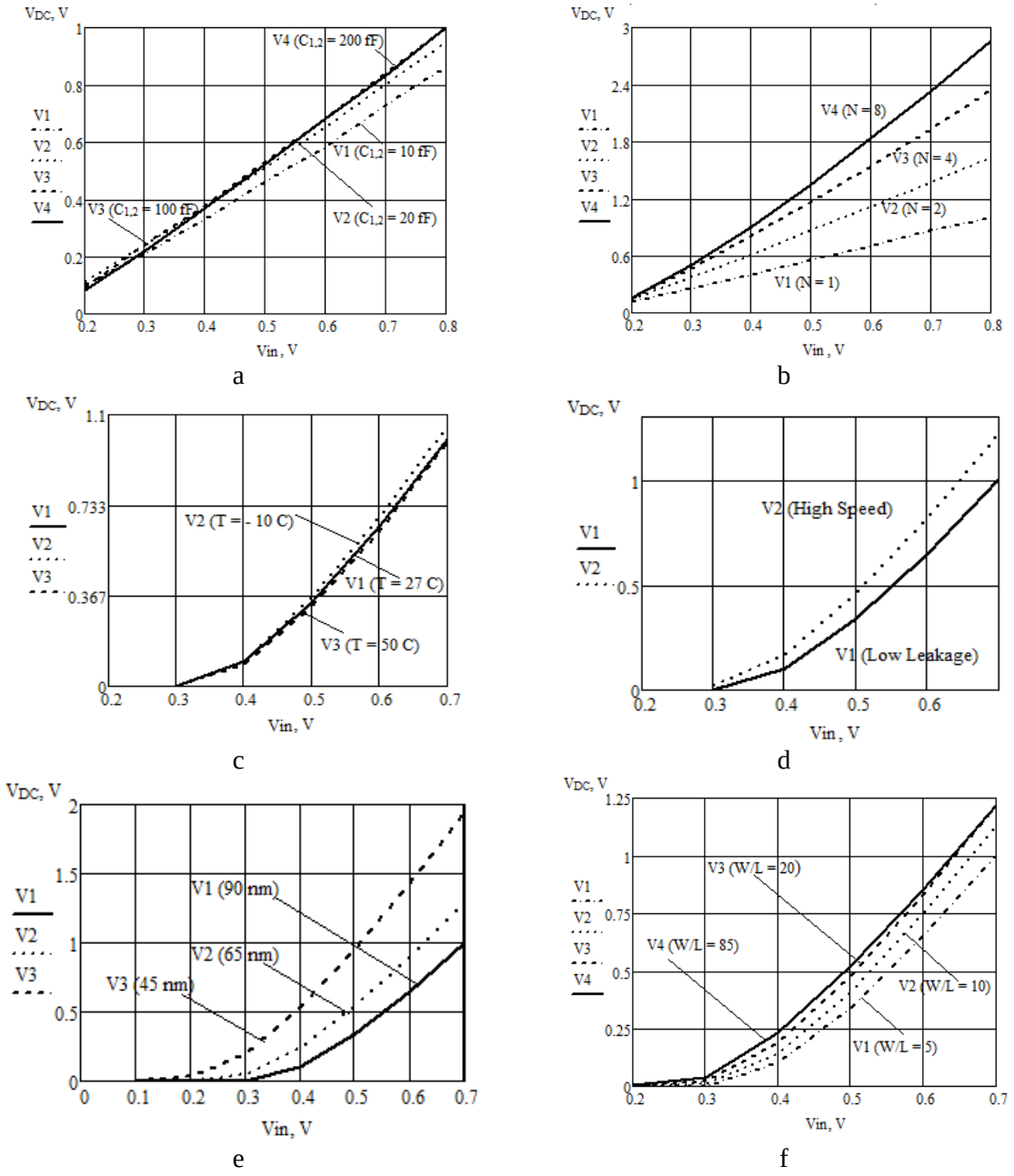

Figure6. *Simulation results of the voltage rectifier. a – the influence of C value on the output voltage of 1-stage circuit; b – the output voltage as a function of number of rectifying stages; c – the output voltage as a function of temperature; d – rectified voltage for different types of transistors, e – the output voltage of rectifier under various design rules; f – alteration of ratio W/L for increasing the output voltage*

During the design of voltage rectifier providing supply voltage for passive radiofrequency tag, in the first place, trials to establish more precise values of capacitance were conducted. The plot of the output voltage versus the input voltage for some values of C is shown in Figure 6a. As can be seen from the figure, when the total capacitance decreases to 20 fF the output voltage level falls and in addition the rectification is not completely carried out. When the capacitance increases to $C_{1,2}$ = 100 fF, the value of rectified voltage is slightly enhances. It has been noted that when the value C_2 is reduced to lower level (30 fF, maintaining C_1 = 100 fF), the output voltage is also increases compared to case of equal capacitances. In the case of further increasing of capacitance (up to 0.5 – 1 pF), the output voltage level doesn't increases and in comparison with the suitable option for single-stage circuit (C_1 = 100 fF, C_2 = 30 fF) even decreases.

The defining of necessary numbers of rectifier stages was the next important step in the design of rectifier. For this, simulation of rectifier circuits with consistently increasing quantity of rectifying cells at constant storage capacitances was conducted, Figure 6b. According to the results of simulation, the rectified voltage reaches required 1.2 V at two stages ($V_{RF} \approx 0.62$ V). For a larger number of cascades, the amplitude of high-frequency sinusoidal signal, at which necessary voltage supply level can be obtained, is respectively lower. However one must take into account that circuit simulation has been conducted so far in the absence of some payload, therefore obtained values of voltage exceed the actual ones.

Based on the results of additional tests, it was found that values of storage capacitances C_1 = 100 fF, C_2 = 30 fF are not suitable for 8-stage rectifier circuit. With a few trials, the acceptable capacitance values were taken equal to C_1 = 200 fF for odd numbers of capacitors and C_2 = 150 fF for even numbers. Further study of rectifier circuit was carried out assuming load resistance is 200 kΩ and number of stages is 8.

Results of the transient simulation of 8-stage rectifier at different temperatures (-10 °C, 27 °C, 50 °C) are shown in Figure 6c. At lower temperature the rectified voltage is several tens of mV higher than the voltage obtained under normal conditions. At high temperatures the output voltage level decreases by approximately 0.01 – 0.02 V compared to normal conditions.

Figure 6d shows comparison of operation of rectifier circuit using different types of MOS transistors. The curve of the output DC voltage in case of use of low-leakage transistors is denoted by a continuous line. The similar response for high-speed transistors is designated by a dashed line. Despite the difference in voltage levels is quite large (0.15 – 0.2 V), significant leakage currents prevent free using of high-speed devices.

In Figure 6e responses of the output voltages obtained for various design rules are shown. According to the study, when technological base 65 nm is used, the output voltage supply (0.7 V for this process) is attained at $V_{RF} \approx 0.55$ V. The rectified voltage supply for process CMOS 45 nm (0.4 V) can be obtained at less than 0.4 V at the input of the rectifier. Suchlike results demonstrate the broad prospects for further researches and developments of radiofrequency devices according to the advanced processes 45 nm and 65 nm.

In order to increase the rectified DC voltage at the output of designed rectifier, the series of tests for enlargement the width of MOS transistors was conducted, Figure 6f. Actually, the ratio W/L was varied while the length of transistor remained unchanged. The ratio of the transistor width to its length in the using technology by default is 5 (W = 0.5 μm, L = 0.1 μm). According to simulation results, each subsequent increasing of ratio W/L (up to 10, 20, 85) enhances the value of rectified voltage, which is natural, since current density in the transistor increases. However for ratio W/L = 10 the output voltage is not sufficient for power supply. The ratio W/L = 85 shows negligible enhancement of the output voltage compared to others variations and extremely high leakage currents (~ 700 nA). An acceptable ratio was W/L = 20 (W = 2 μm) at which the output voltage reaches the desired level of 1.2 V at an amplitude of the input signal less than 0.7 V (leakage current < 100 nA at this ratio). The simulation results of the designed 8-stage rectifier for RFID tag operating at 2.45 GHz are shown in Figure 7.

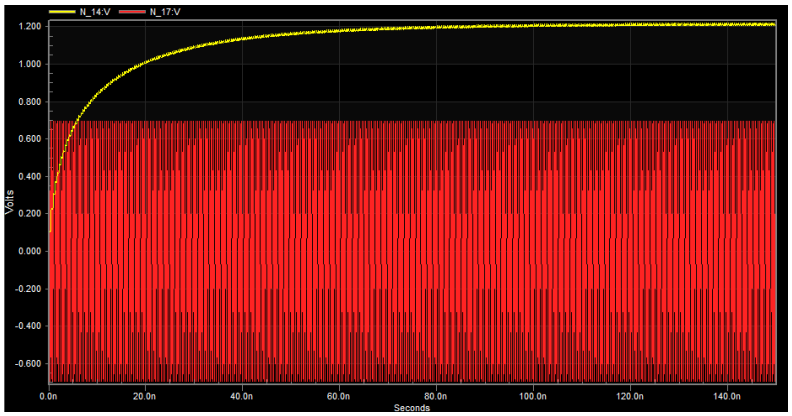

Figure7. *The transient analysis results of the designed 8-stage rectifier with voltage multiplying at input signal amplitude 0.7 V and frequency 2.45 GHz*

The simulation results of proposed reference-voltage source are shown in Figure 8. The rectified voltage arrives to reference-voltage source. The smoothed signal, formed here, with value of 0.42 V serves as the reference voltage in the voltage regulator circuit.

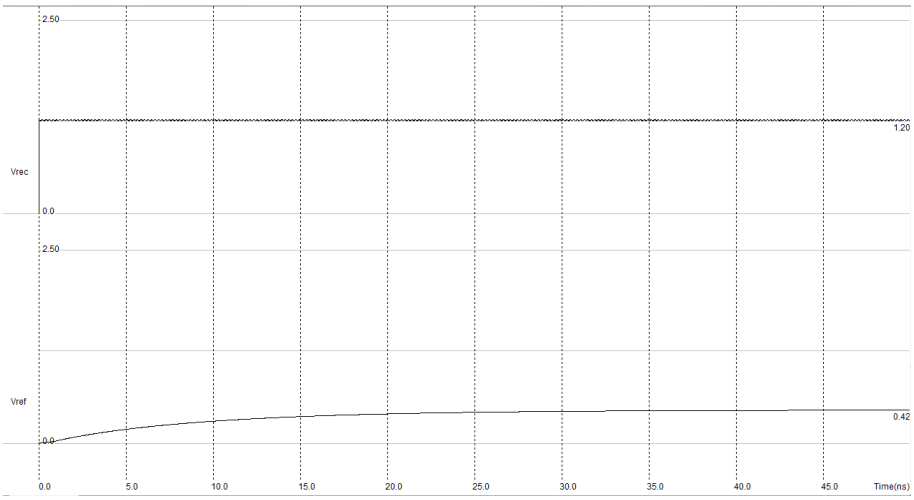

Figure8. *The simulation results of voltage-reference source*

4. CONCLUSION

In this paper the results of comprehensive simulation of the rectifier with charge pumping are presented. The device performance for various values of storage capacitance, number of stages, temperature, size of transistors and other parameters was studied. As a result the rectifier with charge pumping was developed. Diode-connected MOS transistors with enlarged channel width for rectifying the sinusoidal voltage and capacitors for charge accumulation and signal smoothing are used in 8-stage circuit. The layout area of the device, designed for implementation on well-tried 90 nm CMOS technology, is 0.0153 mm^2. The output voltage of the rectifier reaches required 1.2 V to provide power for the rest functional units of the tag at the input signal amplitude less than 0.7 V and frequency 2.45 GHz. In case of using 45 nm technology, it is possible to obtain required supply voltage 0.4 V at much lower input voltages (0.35 V) compared to 90 nm technology, while the operation frequency and the number of stages remain the same. In addition, the layout of reference-voltage to ensure operation of the voltage regulator is proposed.

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