Design of Low Power Efficient Viterbi Decoder

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Abstract: *In communication system encoder and decoder place an important role to detect and correct the errors. Reliability and efficiency of data transmission are the important issues in communication system. Asynchronous circuit consumes less power hence these types of circuit are used more in recent years. Low power chips having more demand in market for portable electronics devices. Electricity generation is the major source for air pollution. The using of low power chips saves power and indirectly shows the concern about environment. In this paper, efficient low power Asynchronous Viterbi decoder is designed and compares the performance parameters with the Synchronous Viterbi Decoder. The convolutional encoder is designed with the constraint length of 4 and code rate of 1/3. Viterbi Decoder having three sub modules are Branch Metric Unit(BMU), Add Compare and Select Unit, and Trace Back Unit(TBU). The Viterbi Decoder algorithm is works based on trellis diagram. Asynchronous design includes clock gating technique to reduce the power consumption. The two designs are designed using Verilog HDL and Simulated using Xilinx 13.1 ISE and implemented on FPGA. The above designs are synthesized using RTL Compiler by generating vcd file.*

Keywords: *convolutional encoder, Branch Metric Unit, Add Compare Select Unit, Trace Back Unit, Trellis Diagram, clock gating.*

1. INTRODUCTION

Communication system is a system which sends information from source to destination. Information or data is represented as binary digits in digital communication system. These bits are corrupted due to the channel noise. Channel coding is used to correct the data in noisy channel. By this technique channel capacity is improved. Convolutional coding and block coding are the two types of channel coding. Convolutional encoder operates on serial data and bock coder operates on block size of the data.

Viterbi decoder is an efficient decoding system for reliable communication system over noisy channel. Viterbi decoders having 3 blocks are Branch MetricUnit (BMU), Add Compare Select Unit (ACSU)and Trace Back Unit (TBU).
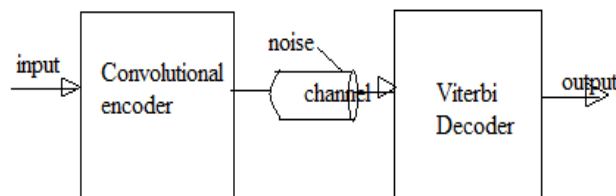

Figure1. *Basic Block Diagram of Convolutional Encoder and Viterbi Decoder*

The name indicates that the coding scheme performs a convolution of the input stream with the encoder's impulse responses. This procedure spreads the bits information over the large sequences which results the increased of transmission redundancy. Convolution encoder operations are performed by using EX-OR gate. Convolutions codes are widely used in following applications are mobile communication, radio communication, anddigital radio.

2. LITERATURE SURVEY

In this section discussed pares related to the proposed design. BineetaSoreng, Saurabh Kumar [1] presented Efficient Implementation of Convolutional encoder and Viterbi Decoder. In this paper

describes about the convolutional encoder and Viterbi decoder. Prof. Siddeeq Y. Ameen, Mohammed H. Al-Jammas and Ahmed S. Alenezi [5] presented FPGA Implementation of Modified Architecture for Adaptive Viterbi Decoder. In this paper aim is to reduce the power and increase the speed. In this the decoder was simulated using MATLAB 7.The adopted design was coded using VHDL and implemented on a SPARTAN 3.Andrew J. Viterbi [2] presented Convolutional Codes and Their Performance in Communication Technology. This includes the fundamental properties and structure to the convolutional encoder. This paper is fundamental to the design of convolutional and Viterbi decoder.

3. CONVOLUTIONAL ENCODER

Convolutional encoder encodes the k bit symbols in to the n bit symbol. It is represented in (n,k,m) format.

- n is the number of output bits of the encoder
- k is the number of input bits to the encoder
- m is the number of memory element of shift registers.

Code rate of convolutional encoder is k/n. Generator polynomial are the mathematical representation of the convolution encoder. Proposed design having three generator polynomials are $G1=1+x+x^2$, $G2=1+x^3$, $G3=1$. Convolutional encoder block diagram is shown in figure.2. It is having four memory elements.one is used to store the input bit xin and three are used to store the previous input bits. The "x" is represent the xin(n-1) and "x^2" represent the xin(n-2) and "x^3" is xin(n-3). Memory element is designed using D Flip Flop. Generator polynomial is designed using simple adder or XOR gate. Depending on the polynomial equation encoder outputs the encoded data. In this deign 8 bit input data is encoded as 24 bit data.
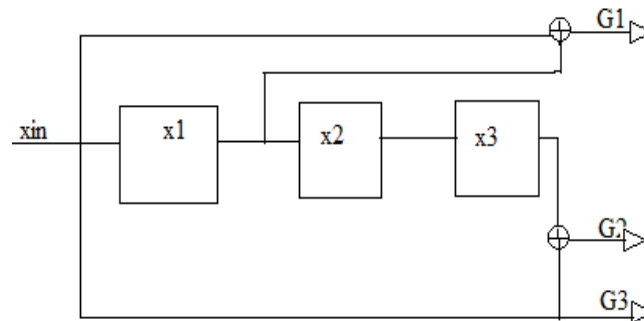

Figure2. *Convolutional encoder*

TABLE1 shows the state table of convolutional encoder, which is consisting of current state, encoded data i.e. output of the convolutional encoder and shifted register value i.e. next state. Encoder will use the input bit with register values to produce output. In figure 2 x1, x2, and x3 are the values stored in the register and G1, G2, G3 are the output values in table 1. The proposed design consisting of eight states values from zero to seven. In this design considered zero is the initial states.

Table1. *State table of convolutional encoder*

Input	Current register value	Encoded output	Shifted register value
0	000	000	000
1	000	111	100
0	001	010	000
1	001	101	100
0	010	001	001
1	010	110	101
0	011	011	001
1	011	100	101
0	100	001	010
1	100	110	110
0	101	011	010
1	101	100	110
0	110	000	011
1	110	111	111
0	111	010	011
1	111	101	111

Trellis diagram shows the operation of the convolutional encoder and it is used to trace back the original data. Trellis diagram for the proposed design is shown in the Figure.3.

In Trellis diagram s0, s1, s2, s3, s4, s5, s6,and s7 represent the states. Depending on the input value state can travel and outputs the data. This data is tabulated in TABLE1. Encode and decode the data by travelling the Trellis diagram. Initial state is always considered as "zero" and it is shown in the trellis diagram for calculation purpose. In figure 3,it travels from state s0 to s0 if input bit is zero or s0 to s4 if input bit is one, similarly s2 to s1 if input is zero else s2 to s5, s4 to s2 if input is zero else s2 to s6, and it continues depending on the state values and input bit. This trellis diagram having the total 94 branch metric values. Depending on the present and next state and cycle value named the branch metric for easy to identify. Example b000 indicates that initial stage, present state is zero and next state is zero, similarly b104, stage1, present state is 0 and next state is four etc.
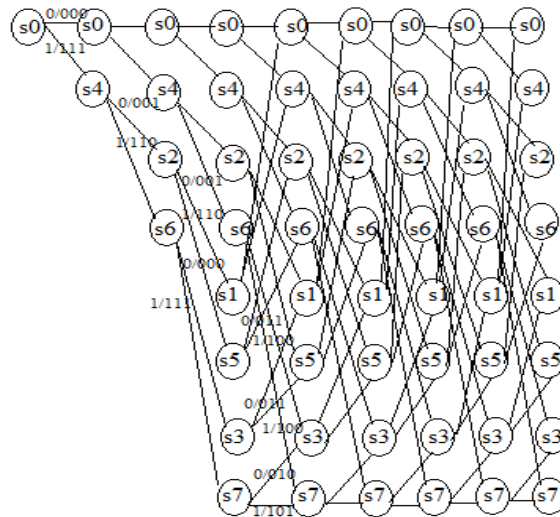

Figure3. *Trellis Diagram*

4. VITERBI DECODER

Viterbi decoder was designed using Viterbi algorithm. Viterbi algorithm will do maximum likelihood decoding algorithm. Disadvantage of this decoder is consuming more resources. It is suitable for constraint length is less than ten. If constraint length more than ten complexities is increases and size of the trellis diagram increases.

 Viterbi decoder having three blocks namely

- Branch Metric Unit(BMU)
- Add Compare Select Unit(ACSU)
- Trace Back Unit(TBU)

This paper having two proposed design are Design-I and Design-II. Design-I is Synchronous Viterbi Decoder and Design-II is asynchronous Viterbi Decoder. Both the design having common BMU, ACSU and TBU blocks.

A.Design-I

Design-I is decode the encoded data by using common control signal. This design is shown in the Figure 4. It is the synchronous circuit.
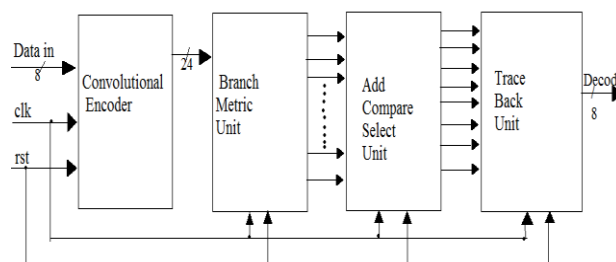

Figure4. *Block diagram of Design-I*

Branch Metric unit works by calculating the hamming distance. Add compare select unit calculates the path metric which is used to trace back the original data. Trace back unit trace the original input data by using path metric.

B. Design-II

Design-II is an asynchronous Viterbi decoder. Clock signals are generated depending on the control signal generated by each block. In this design clock gating technique is used to reduce the power dissipation. By using clock gating we can supply the clock when that block is needed. Clk1, clk2, and clk3 are the clocks generated using clock gating technique. In this design only one clock supply is enough to operate because using of the clock gating technique. Design of BMU, ACSU and TBU is similar to design-I exceptusing and generation of control signals. Figure 5 shows the architecture diagram of Design-II.
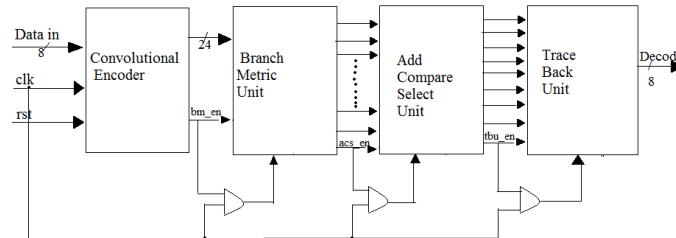

Figure5. *Block Diagram Of Design-II*

The signal clk1 is generated by clk logical AND with bm_en, clk2 is generated by clk logical AND with acs_en and clk3 is generated by clk logical AND with tbu_en. In Design-II only 3 additional AND gate is required this will results in reducing power.

5. SIMULATION RESULTS OF CONVOLUTIONAL ENCODER, BMU, ACSU, TBU, DESIGN-I, AND DESIGN-II

Convolutional Encoder having 8 bit input data and 24-bit encoded data. This block encode the one bit input data at a time and produce 3 bit encoded data represented by G. Figure 6 shows the simulation result of the Convolutional Encoder.Applied input is "10101101".
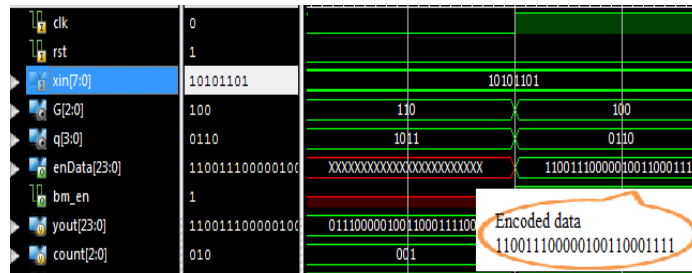

Figure6. *Simulation result of Convolutional Encoder*

The Branch Metric Unit is designed to calculate the hamming distance between the received data and expected data. Figure 7 shows the simulation result of the Branch metric unit. It is having 94 branch metric output values, here showing olnly some of the values.
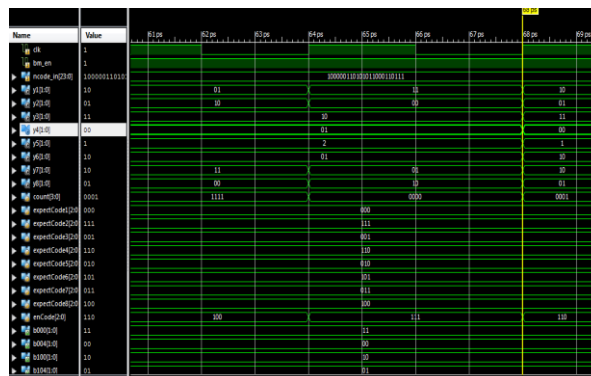

Figure7. *Simulation Result of Branch Metric Unit*

ACSU outputs the path metric value which is shown in the Figure 8.These path metric values are given to the Trace Back Unit as input.Figure 8 shows the eight state path metric values.
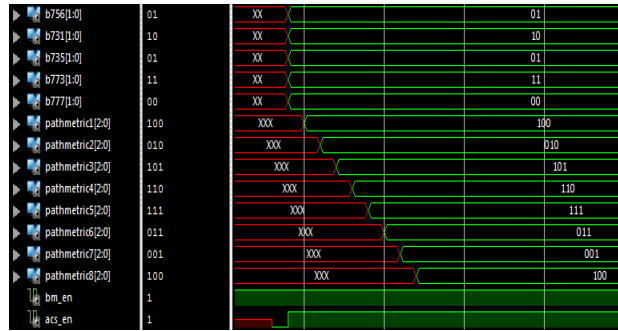

Figure8. *Simulation Results of Add Compare Select Unit*

Trace Back Unit is works based on the Trellis diagram. Inputs for the Trace Back Unit are the state path metric values from the ACSU. Figure 9 shows the simulation result of the trace back unit.Decode_out is the eight bit output data in figure 9.
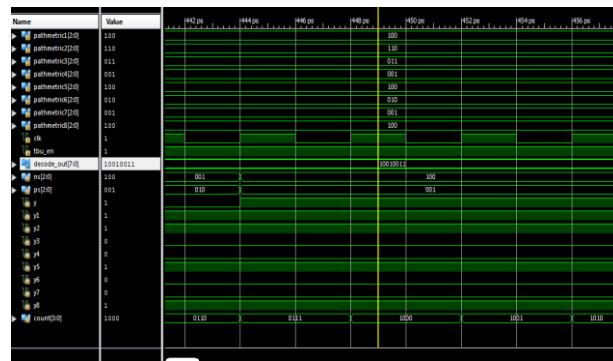

Figure9. *Simulation results of the Trace Back Unit*

Design-I is based on the synchronous circuit. Figure 10 shows the RTL Schematic of the Design-I and Figure 11 shows the simulation result of the Design-I. xin is the 8-bit input data, decode_out is the 8-bit decoded data. In Figure 10xin is 10011101 is the input data and this design is able to get back the same data. Design-II is having same Convolutional Encoder, BMU, ACSU and TBU blocks.
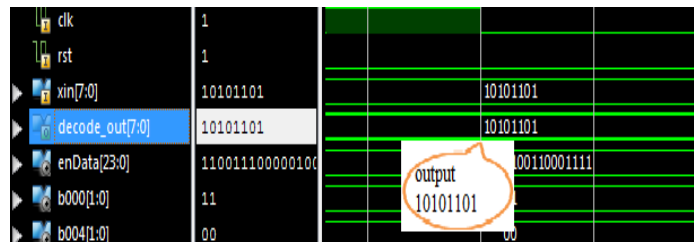

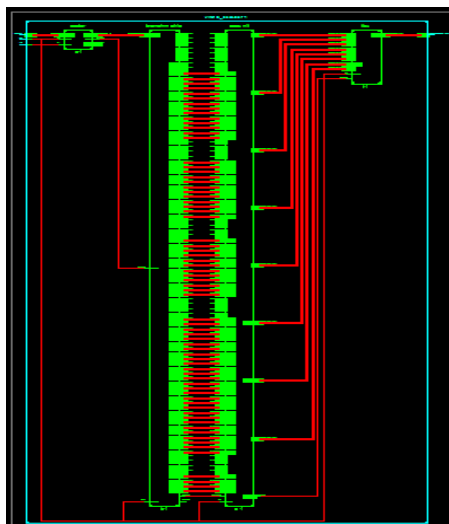**Figure10.** *Simulation result of Design-I*

Figure11. *Detailed RTL Schematic of the Design-I*

Design-II having four different clock signals are clk,clk1,clk2 and clk3. Clk1, clk2, and clk3 are generated depending on bm_en, acs_en and tbu_en control signal using clock gating technique. It is an asynchronous design. Figure 12 shows the simulation result of the Design-II. Figure 13 shows the Detailed RTL Schematic of the Desihn-II.
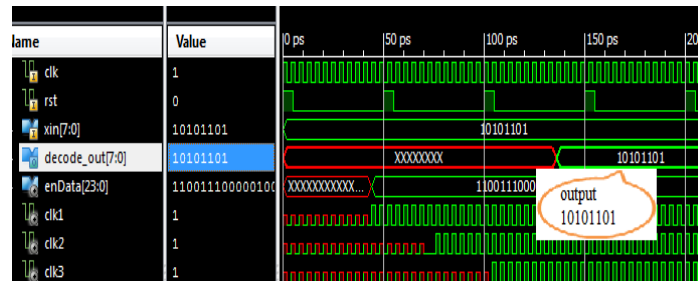

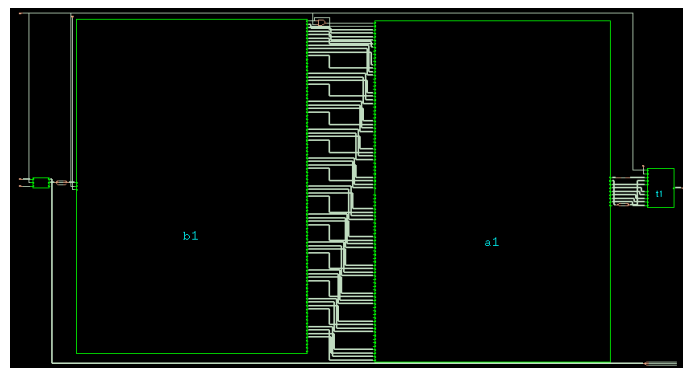**Figure12.** *Simulation Result Of Design-II*

Figure13. *Detailed RTL Schematic of the Design-II*

6. SYNTHESIS REPORT OF DESIGN-I AND DESIGN-II

Table-2 shows the power report of the Design-I and Design-II. This result can be achieved by adapting simple clock gating technique in Design-II.Table-3 consisting of total area used by both the design and comparison of the both the design.

Table2. *Power report comparision table of the design-i and design-ii*

Parameter	Design-I	Design-II	Percentage Change
Leakage Power(nW)	10658.191	10661.615	0.03% Increase
Dynamic Power(nW)	74398.410	64390.005	13.45% decrease
Total Power(nW)	85056.601	75051.621	11.76%decrease

Table3. *Area report of the design-i and design-ii*

Parameter	Design-I	Design-II	Percentage Change
Cells	518	519	0.19% increase
Cell area	3174	3178	0.12% increase

7. CONCLUSION AND FUTURE WORK

In this paper have two designs. One is synchronous Viterbi decoder and another one asynchronous Viterbi decoder. From Table2 and Table-3, small increase in area we have achieved that 11.76% reduction in power without changing sub module design.

In future by applying various power reduction techniques we can minimize the power utilization further. Implement this design on FPGA and see the result using Chip Scope Pro analyzer.

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