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Introducing 55-Level ACMLIs with Very Low Harmonics Values Over Wide Voltage Ranges

M. El-Bakry

Electronics Research Institute, Egypt
mahmdali42@yahoo.com

Abstract: *This paper considers single phase and three phase 55-level asymmetric cascaded multilevel inverters (ACMLIs), that consist of four H-bridges per phase, with dc sources E, 3E, 9E and 14E , where E is an arbitrarly chosen reference dc voltage value. An approach using a mixed integer linear programming (MILP) model is introduced to determine the switching angles of the inverter power switches that minimize the values of any undesired harmonics. The model is solved first to determine the number of harmonics to be minimized to obtain least value of the exact total harmonic distortion (%THDE) and least value of any undesired harmonic between all harmonics from the low order harmonics till the 199th harmonic relative to the main harmonic (%V $_{LH)}$ for an output voltage that is formed from all the 55 levels of the inverter. Then the model is solved aiming minimizing these harmonics for different output voltage amplitudes. For single phase case, output voltages amplitudes between 14E and 28E could be obtained with %V $_{LH}$ less than 1%, and between 20E and 28E with % V $_{LH}$ less than 0.5%. For three phase case, output phase voltages amplitudes between 12E and 32E could be obtained with %V $_{LH}$ less than 1 % and between 18E and 30E with %V $_{LH}$ less than 0.5%. In addition, the obtained values of %THDE and %V_{Hmax} agree with the IEEE standards 519-1992 for voltage distortion limits till 161kv for both single and three phase cases over wide voltage amplitude ranges.*

Keywords: *Cascaded Multilevel Inverters; Exact Total Harmonic Elimination; Harmonic Values Minimization; Mixed Integer Linear Programming.*

1. INTRODUCTION

Recently the multilevel inverter (MLI) is the most popular dc to ac converters topology for high voltage and high power in the power systems. The MLI synthesize a sinusoidal voltage from several levels of voltages. There are three well known topologies; diode-clamps, flying capacitor, and cascaded multilevel inverter (CMLI). CMLI had many advantages than others, especially in reduced component, reduced power loss, reduced power stress, reduced frequency switching, reduced electromagnetic interference, increase voltage and power capability and increase power quality. In the early development, all of H-bridge inverters of CMLI have same value of dc voltage, and the CMLI called symmetric CMLI (SCMLI). But in order to improve the power quality with a large number of output levels without increasing the number of inverter H-bridges, unequal dc voltages or asymmetric cascaded multilevel inverters (ACMLIs) are built, where each H-bridge of its inverter has different value of dc voltage [1]. Recently, ACMLIs have received special attention [2, 3, 4].

The ACMLI synthesizes a desired sinusoidal voltage from several separate dc voltage sources. The general construction of the ACMLI is shown per phase in Fig. 1. It consists of a number of H-bridges fed with dc voltages sources E_1, E_2, .. and E_S .The output voltage is usually constructed in a staircase shape, Fig. 2, to approach synthesizing a sinusoidal wave form, [5].

In an ACMLI the dc sources are of unequal values. In this case the maximum number of the positive levels of the inverter can be increased greatly, since it could be possible to switch on some dc sources positively or negatively within the positive time half cycle of the output voltage, thus adding additional positive levels. Generally, the possible positive levels of an ACMLI are all the positive values of $I_1 E_1 + I_2 E_2 + \ldots + I_S E_S$, where each of I_1, I_2, .. and I_S can take one of the values -1, 0 or +1. The number of all possible levels is $(3)^s$, some of them may be redundant. Increasing the levels of the inverter means that its staircase output wave form can approach more closely a sinusoidal wave form, which in turn means that the undesired output voltage harmonic values and their total harmonic distortion could be reduced greatly, and this make ACMLIs more popular for many practical applications [6].

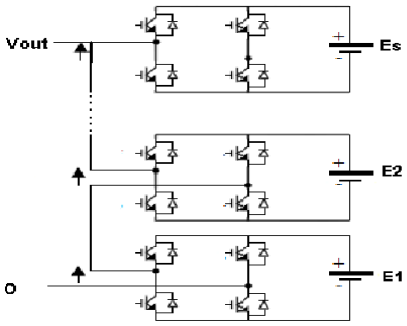

Fig1. *A single phase cascaded multilevel with S dc sources*

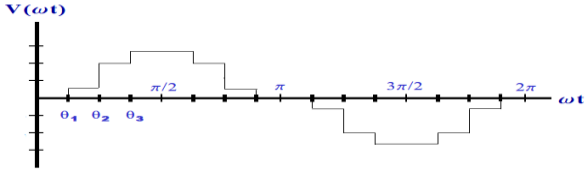

Fig2. *A staircase output voltage wave form with 3 positive levels*

To obtain a staircase output voltage wave form with equal step heights in an ACMLI, the following uniform step sufficient conditions may be satisfied by the dc sources E_1, E_2, . . and E_S, [6]:

1- $E_1 \leq E_2 \ldots \leq E_S$, $E1 < E_S$, and each of E_2, E_3, . . , and E_S is an integer multiple of E_1.

2- $E_J \leq E_1 + 2 \sum_{r=l}^{r=J-1} E_r$, and J = 2, . . , S

It is possible to obtain the maximum number of levels in an ACMLI, i.e. $(3)^s$ non-redundant or different levels, by replacing the inequality sign in the second condition with an equality sign. .Thus with $E_1 = E$ we get $E_2 = 3E$, $E_3 = 9E$. By adding a fourth H-bridge with $E_4 = 14E$, that satisfies the second condition, an ACMLI could be constructed with a 27 uniform step positive levels: E, 2E, 3E,.. ..and 27E , and with a total number of 55 levels. Different alternatives are possible to obtain these 27 positive levels during the quarter time cycle of the output voltage. The best alternative is to switch the low voltage dc sources E_1 and E_2 positively or negatively with E_3 and E_4 and thus reducing the switching losses.

Modern methods proposed in the literature for determining the switching angles of the power switches of ACMLIs depend mainly on pulse width modulation (PWM) techniques, [7,8,9], but these are not suitable for an ACMLI with large number of levels.

In this paper the 55-level ACMLI is considered, and an approach depending on mixed integer linear programming for determining the switching angles of this inverter that minimize any values of undesired harmonics is introduced and applied for single phase and three phase ACMLIs.

2. A Proposed Approach for Determining the Switching Angles of the ACMLI

A fundamental issue for an ACMLI is to find the switching angles (times) of the inverter H-bridges semiconductor power switches that produce the required fundamental voltage and at the same time eliminate or reduce the values of undesired specific harmonics.

The author has introduced a method based on a mixed integer linear programming (MILP) model that could be applied here to minimize the values of any undesired harmonics, [10]. This MILP model has the following advantages over other methods discussed in the literature:

- This model is flexible. It allows minimizing the values of harmonics of any order and any number, independent of the number of inverter levels, under any required possible value of the main harmonic.

- MILP constraints could be inequality constraints, so a feasible solution can be almost found, unlike harmonic elimination method equations which may give no feasible solution due to the trigonometric nature of the problem.
- MILP constraints allow minimizing harmonics values with different weighting factors according to the harmonic order. Low order harmonics values could be minimized much more than higher order ones.
- MILP provides global optimal solution of the problem over the whole solution space, unlike some other optimization methods that give a local optimal solution near an initial solution, which may not be a global optimal solution.
- Many software packages are available for solving MILP models, even with huge number of variables and constraints, in a moderate time. They are suitable for large problems that could not be easily solved with other methods.
- The model can be applied even for ACMLIs with non uniform steps by adding additional constraints, [11].
- The model contains many parameters that could be selected arbitrarily. Many optimum solutions could be obtained for the same problem corresponding to different values of these parameters, and thus allowing for selecting the best one.

The mathematical model of this approach is first given, and then applied for single phase and three phase 55-level ACMLI. The model is applied first to determine the number of harmonics to be minimized that leads to least %THDE and % V_{LH} at an output voltage that is formed from all the 55 levels of the ACMLI. By including this result in the model and solving it for different amplitudes of the output voltage, the switching patterns that probably give least values % THDE and % V_{LH} are obtained.

3. THE PROPOSED MATHEMATICAL MODEL

A general uniform step SCMLI, or an ACMLI, with a step height E is considered, where all the inverter levels are spaced equally. It is assumed, without loss of generality, that the inverter levels are equally spaced by 1 volt, i.e. normalized with respect to the reference dc voltage E. It is assumed also that the inverter output voltage wave form F(wt) is an odd-sines periodic function, as that shown in Fig. 2. The pattern of this function is generated by on and off switching of the inverter H-bridges semiconductor power switches, and is completely determined by defining the switching pattern over the interval $0 \le wt \le \pi/2$. The basic approach depends on dividing this interval into N equal small subintervals, starting at the angles $0, \tau, 2\tau, \ldots, (I-1)\tau, \ldots$ till $(N-1)\tau$., where $\tau = \pi/2N$, Fig.3.

The positive integer values X_I, I=1, 2, . . , N are defined over each subinterval, to represent the required instantaneous output voltage level value F(wt) of the inverter, so that F(wt) is defined over the interval $0 \le wt \le \pi/2$ by:

$F(wt) = X_I$ for $(I-1)\tau \le wt \le I\tau$ and I=1,2,..,N

The odd-sines Fourier series expansion of F(wt) is given by:

$$F(wt) = \sum_{m=0}^{m=\infty} V_{2m+1} \sin(2m+1)wt \text{ , where}$$

$$V_{2m+1} = (4/\pi) \int_0^{\pi/2} F(wt) \sin(2m+1)wt \, dwt$$

$$= (8/\pi(2m+1)) \sum_{I=1}^{I=N} X_I \sin(2m+1)\tau/2 \sin(2m+1)(\theta_I+\tau/2) \quad (3.1)$$

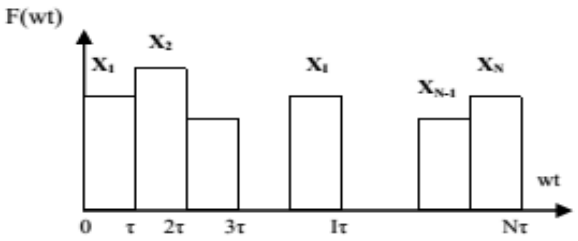

Fig3. *Representation of F(wt) by X_I, I= 1, 2, … ,N over the interval $0 \le wt \le \pi/2$*

where (2m+1) is the order of the harmonic , m= 0,1, 2, . . .,∞, $\tau = \pi/2N$, and $\theta_I = (I-1)\tau$.

The value of the amplitude of main harmonic corresponds to V_1, i.e. by substituting m=0 in equation (3.1).

Equation (3.1) shows that V_{2m+1} for any value of m is a linear function of the integer values X_I, I=1,2, . ., N. Variations of the values of X_I from a subinterval to a next one determine the required switching angles of the inverter from one level to another.

It is required to find the values of X_I that minimize the values of some undesired harmonics. A mixed integer linear programming (MILP) problem is formulated as follows, [11]:

Minimize ε, subject to the constraints:

$$* \; V'_1-\Delta \le V_1 \le V'_1+\Delta \tag{3.2}$$

$$* \; -\varepsilon \, \alpha_{2m+1} \le V_{2m+1} \le \varepsilon \, \alpha_{2m+1}, \text{ for each undesired harmonic of order } (2m+1) \tag{3.3}$$

$$* \; X_I \le X_{I+1}, \text{ for I= 1,2, . . , N-1, and } X_N \le L \tag{3.4}$$

$$* \; X_I \ge 0 \text{ and integer for I=1, 2, . . , N} \tag{3.5}$$

In constraint (3.2) V'_1 is the required amplitude of the main harmonic, and Δ is a small incremental value, $\Delta << V'_1$, arbitrary chosen and added to the main harmonic constrain to ensure obtaining an optimum solution, since an equality constraint may give a high value of ε or even an unfeasible solution., due to the trigonometric nature of the constraints. The value of Δ is taken of the order of 3 % of V'_1, so that they obtained value of V_1 does not differ practically from the required value of V'_1.

In constraints (3.3) V_{2m+1} is given by equation (3.1), for V_1 and the undesired harmonics, and α_{2m+1} is a weighting factor for the undesired harmonics, to enable reduction of harmonics with different upper bounds according to their order.

By constraints (3.4) the positive staircase wave form shape is assured with maximum height L, where L is the maximum probable number of positive voltage levels of the inverter.

Constraints (3.5) are the integer constraints on X_I.

Once all the parameters of this MILP model are given, an optimum solution could be obtained that gives the values of X_I and ε using any of the well known operations research software packages, e.g. "LINGO" software [12].

When solving this MILP model, it will include formulas for calculating the exact total harmonic distortion (%THDE), the maximum value of any undesired harmonic between all undesired harmonics from the low order harmonics till the 199th harmonic relative to the main harmonic ($\%V_{LH}$) and the upper limit of the amplitude of any undesired harmonic relative to the amplitude of the main harmonic ($\% V_{Hmax}$). These formulas are given in the next section.

4. Formulas for Calculating %THDE, $\%V_{LH}$ and $\%V_{HMAX}$ of the Output Harmonics

4.1. The Formulas for Calculating the %THDE

The exact total harmonic distortion (%THDE) including all possible undesired harmonics is given by:

$$THDE = [\sum_{m=1}^{m=\infty} \{V_{2m+1}/V_1\}^2]^{0.5} \tag{3.6}$$

The value of THDE could be obtained from the solution of the MLIP model, after obtaining the values of X_I using the following expressions, [13]:

- For single phase CMLI, the output phase voltage THDE is given by:

$$THDE = [\{(1/N) (\sum_{I=1}^{I=N} X_I^2) / V_{1rms}^2\} - 1]^{0.5} \tag{3.7}$$

- For a balanced three phase ACMLI, the output phase voltage THDE is given by, assuming that N is a multiple integer of 3, [13]

$$THDE = [\{(1/2N)\ (\sum_{I=1}^{I=2N} Z_I^2) / V_{1rms}^{\ 2}\}-1]^{0.5} \quad (3.8)$$

where:

$Z_I = X_I - Y_I$ for I=1, 2,.., N

$Z_I = XX_I - YY_I$ for I=N+1,..,2N

$Y_I = - X_{(2N/3)+1}$ for I=1, 2, ..,N/3

$Y_I = -X_{(4N/3)-1}$ for I=(N/3) +1, ..,N

$XX_I = X_{2N+I-1}$ for I= N+1, ..,2N,

$YY_I = - X_{(4N/3)+I-1}$ for I= N+1, ..,4N/3

$YY_I = X_{I—(4N/3)}$ for I= (4N/3)+1, ..,2N

4.2. The Formula for Calculating $\%V_{LH}$ and $\%V_{HMAX}$

To calculate the upper limit of the amplitude of any harmonic among all the undesired harmonics relative to the amplitude of the main harmonic ($\%\ V_{Hmax}$), the MILP model is programmed to calculate first the amplitude of the harmonics V_{2m+1} till the 199th harmonic, i.e. till m = 99 , then the following values are calculated:

- The maximum amplitude value among all the undesired low order harmonics till the 199th harmonic (V_{LH}) relative to the amplitude of the main harmonic:

$$V_{LH} = \max_{m=1,\ldots,99} (V_{2m+1} / V_1) \quad (3.9)$$

- The total harmonic distortion (%THD 199) of the low order harmonics calculated till the 199th harmonic:

$$THD_{199} = [\sum_{m=1}^{m=99} \{V_{2m+1} / V_1\}^2]^{0.5} \quad (3.10)$$

- The rout of the sum of squares of the amplitudes of all the high order harmonics above the 199th harmonic relative to the square of the amplitude of the main harmonic (V_{HH}) is calculated by using the expression :

$$V_{HH} = [THDE^{\ 2} - THD_{199}^{\ 2}]^{0.5} \quad (3.11)$$

From (3.9) and (3.11) an upper limit of the amplitude of any harmonic among all the undesired harmonics relative to the amplitude of the main harmonic (V_{Hmax}) may be given by:

$$V_{Hmax} = \max (V_{LH}, V_{HH}) \quad (3.12)$$

In the following sections all the voltage values are normalized w.r.t. the reference dc voltage E., and the MILP model is applied for 55- level ACMLI assuming the following:

- Taking the number of subintervals N=720. This corresponds to a subinterval angular width of $90^\circ/720 = 0.125^\circ$.
- The model is solved minimizing all undesired harmonics equally, i.e. taking in constraint (3.3) the values of $\alpha_{2m+1} = 1$ for all undesired harmonics.
- First the MILP model constraint (3.2) is replaced by:

$V_1 \geq L$ (3.2')

By this way, the MILP model considers an output voltage amplitude that exceeds the number of the positive levels of the ACMLI and thus the output voltage is formed from all the 55 levels of the ACMLI. The model is then solved to minimize low order harmonics till a harmonic of order k, for different values of k, and selecting the value of k that leads to least %THDE and $\%\ V_{LH}$, as given by the equations in section IV.

- Then the MILP model is solved, using this value of k, to minimize low order undesired harmonics till the kth harmonic for different values of the required output voltage V' using the constraint (3.2) and taking $\Delta = 1$.

By these procedure, the switching patterns of the inverter obtained at different values of the output voltage are expected to give minimize the values of low order harmonics till the kth harmonic with least %THDE and % V_{LH}. These procedures are carried out next for single phase and three phase ACMLIs.

5. Solution of the Model for A 55-Level Single Phase ACMLI

5.1. Solution for Different Values of Undesired Harmonics

Figure 4 shows the values of % THD199,% THDE, % V_{LH} and % V_{Hmax} obtained by solving the model, with the voltage constraint (3.2') replacing the constraint (3.2) with L=27, to minimize the odd harmonics till the kth harmonic for different values of k. The least %THDE and % V_{LH} are obtained by at k=61, i.e. by minimizing the low order harmonics equally till the 61st harmonic.

5.2. Solution for Different Values of the Output Voltage

The model is solved to minimize the undesired low order harmonics till the 61st harmonic for some values of V_1' between 10 and 29 and taking Δ =1. Fig. 5 shows the obtained values of % THD199. % THDE, % V_{LH} and % V_{Hmax}. It is noted that:

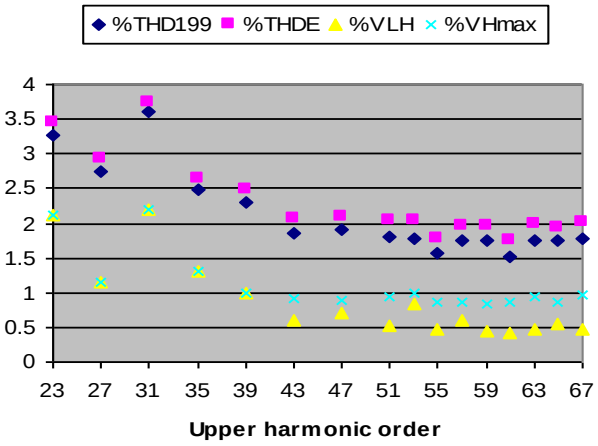

Fig4. *The values of %THD199, %THDE, %VLH and %V_{Hmax} for different minimized harmonics*

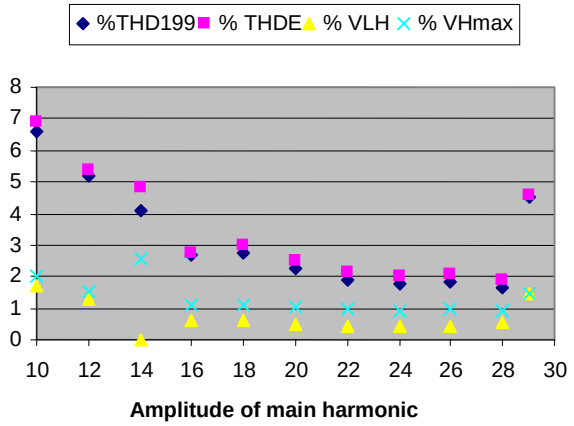

Fig5. *The values of % THD199, %THDE, %VLH and %V_{Hmax} for different values of V'_1*

**The value of % V_{LH} is less than 1% for all output voltages between 14 and 28, and less than 0.5% for all output voltages between 20 and 28.

**The value of % THDE is less than 5%, and the value of % V_{Hmax} is less than 3% for all output voltages between 14 and 29, which agree with the IEEE standards 519-1992 for voltage distortion limits for output voltages $\leq$ 69 kv., [14]

** The value of of % THDE is less than 2.5%, and the value of % V_{Hmax} is less than 1.5% for all output voltages between 20 and 28, which agree with the IEEE standards 519-1992 for voltage distortion limits for output voltages between 69kv and 161kv, [14].

In the following, the detailed solutions are given for V_1' =14, 20 and 28.

For V'_1 =14 the values of V_1 =14.25 %, THD199 = 4.09%, THDE = 4.82%, % V_{LH} = 0.95 and % V_{Hmax} = 2.56 %. For this value of V_1, Fig. 6 shows the obtained values of X_I. Fig. 7 shows the obtained percentage values of the harmonics relative to the main harmonic from the 3rd till the 199st harmonic, and a 2% of the main harmonic.

For V'_1 =20 the values of V_1 =19.18, %THD199 = 2.25%, THDE = 2.48 %, % V_{LH} = 0.49 and of % V_{Hmax} = 1.04 %. For this value of V_1, Fig. 8 shows the obtained values of X_I . Fig. 9 shows the obtained percentage values of the harmonics relative to the main harmonic from the 3rd till the 199st harmonic, and a 2% of the main harmonic.

For V'_1 =28 the values of V_1 =27.12 %, THD199 =1.64 %, THDE = 1.88 %, of % V_{LH} = 0.56 and of % V_{Hmax} = 0.91 %. For this value of V_1, Fig. 10 shows the obtained values of X_I. Fig. 11 shows the obtained percentage values of the harmonics relative to the main harmonic from the 3rd till the 199st harmonic, and a 2% of the main harmonic.

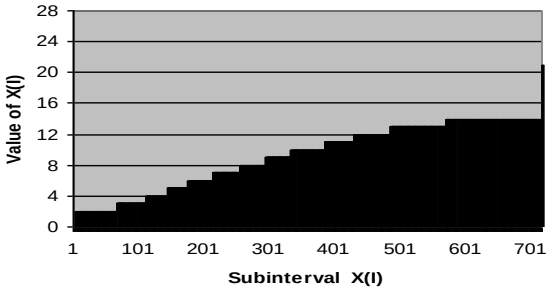

Fig6. *Values of X_I that give V_1 = 14.25*

Figure 12 shows the switching pattern of the four H-bridges of the inverter during the positive quarter time cycle of the main harmonic at V_1 =27.12. The 1E H-bridge and the 3E H-bridge are switched on and off positively and negatively several times, while the 9E H-bridge is switched positively two times on and one time off, the 14E H-bridge is switched positively on one time.

The multiple switching of the power switches is done only for the low voltage power switches at lower switching losses, and this does not represent any serious problem, specially with recent development of semiconductor power switches that operate at high frequencies with low switching losses, [15].

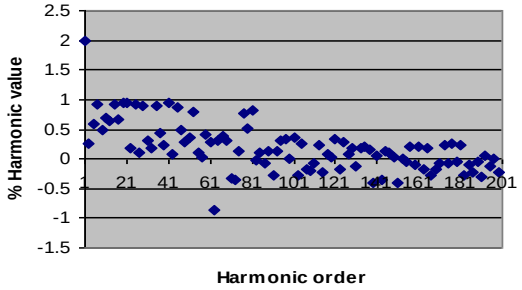

Fig7. *% Values of undesired harmonics for V_1 =14.25*

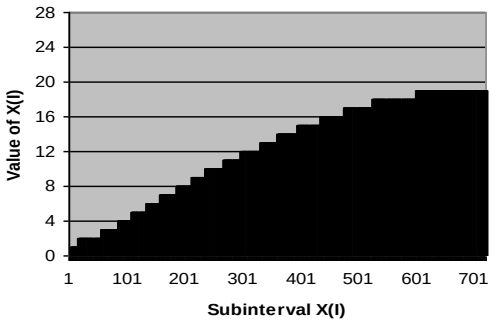

Fig8. *Values of X(I) that give V_1 = 19.18*

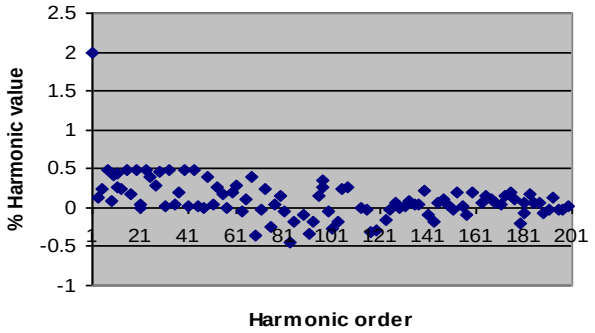

Fig9. *%Values of of undesired harmonics for V_1 =19.18*

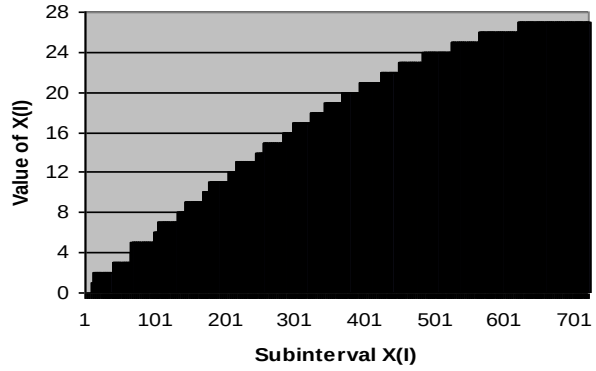

Fig10. *Values of X(I) that give V_1 = 27.12*

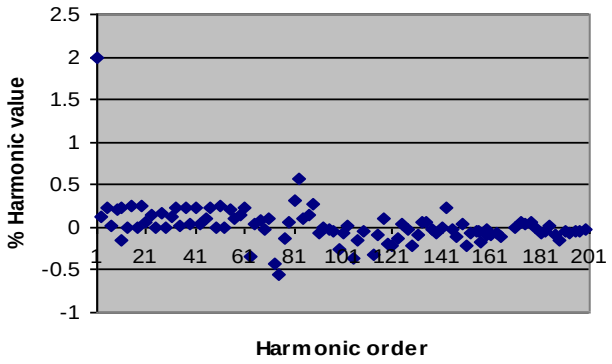

Fig11. *% Values of undesired harmonics for V1 = 27.12*

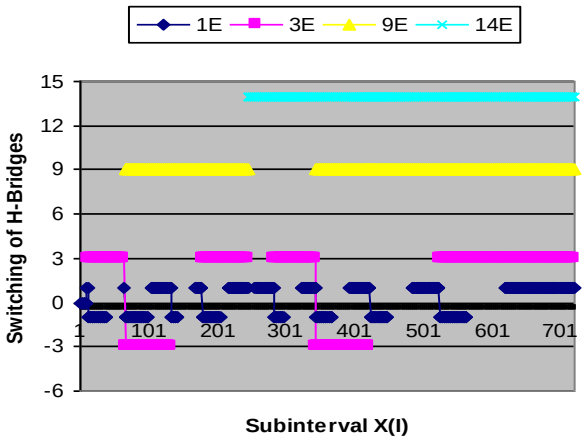

Fig12. *Switching pattern of the H-bridges for V1 = 27.12*

6. SOLUTION OF THE MODEL FOR A 27-LEVEL THREE PHASE ACMLI

In a balanced three phase operation the triplen odd harmonics, i.e. the 3rd, 9th, 15th,. .and so on, are self cancelled in the output line voltage assuming a star connected three phase inverter. The procedure carried out in section V with single phase asymmetric CMLI is repeated with excluding the triplen odd harmonics, as follows:

6.1. Solution for Different Values of Undesired Harmonics

Figure 13 shows the values of % THD199,% THDE, % V_{LH} and % V_{Hmax} obtained by solving the model, with the voltage constraint (3.2') replacing the constraint (3.2) with L=27, to minimize the non-triplen odd harmonics till the kth harmonic for maximum output voltage at different values of k. The least %THDE and % V_{LH} are obtained by at k=61, i.e. by minimizing the low order harmonics equally till the 61st harmonic.

6.2. Solution for Different Values of the Output Voltage

The model is solved to minimize the undesired low order harmonics till the 61st harmonic for some values of V_1' between 10 and 29 and taking Δ =1. Fig. 14 shows the obtained values of % THD199. % THDE, % V_{LH} and % V_{Hmax}. It is noted that:

**The value of % V_{LH} is less than 1% for all output voltages between 12 and 32, and less than 0.5% for all output voltages between 18 and 30.

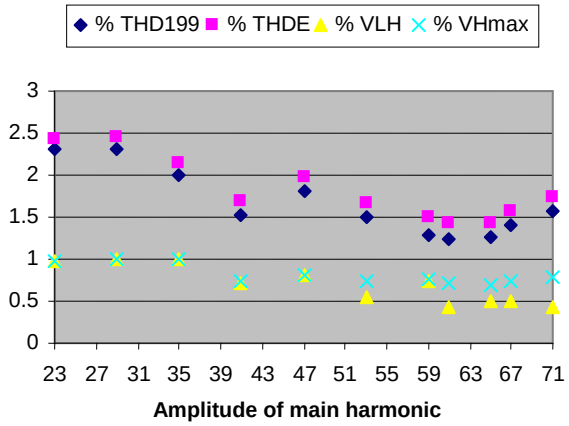

Fig13. *The values of % THD199, %THDE, %VLH and %V_{Hmax} for different values of V'$_1$*

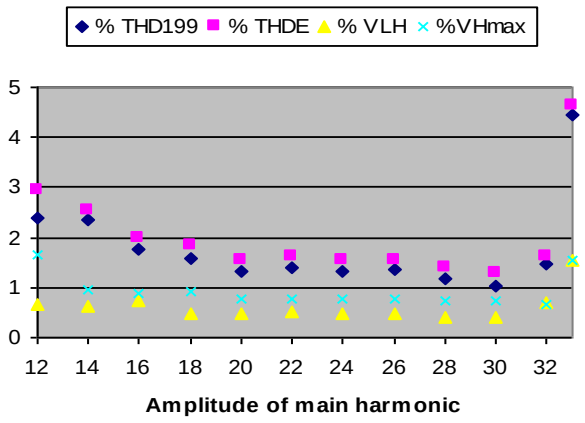

Fig14. *The values of % THD199, %THDE, %VLH and %V_{Hmax} for different values of V'$_1$*

** The value of of % THDE is less than 2.5%, and the value of % V_{Hmax} is less than 1.5% for all output voltages between 16 and 32, which agree with the IEEE standards 519-1992 for voltage distortion limits for output voltages between 69kv and 161kv., [14].

In the following, the detailed solutions are given for V_1' =16, 24 and 30.

For V'_1 =16 the values of V_1 =16.22, %, THD199 = 1.77, % THDE = 1.97%, % V_{LH} = 0.74 and % V_{Hmax} =0.88 %. For this value of V_1, Fig.15 shows the obtained values of X_I. Fig.16 shows the obtained percentage values of the harmonics relative to the main harmonic from the 3rd till the 199st harmonic, and a 2% of the main harmonic

For V'_1 =24 the values of V_1 24.26, %THD199 =1.33 % THDE =1.55 %, % V_{LH} = 0.49 and of % V_{Hmax} = 0.79 %. For this value of V_1, Fig.17 shows the obtained values of X_I. Fig. 18 shows the obtained percentage values of the harmonics relative to the main harmonic from the 3rd till the 199st harmonic, and a 2% of the main harmonic.

For V'_1 =30 the values of V_1 =29 % THD199 =1.03 % THDE = 1.27 %, of % V_{LH} = 0.39 and of % V_{Hmax} = 0.73 %. For this value of V_1, Fig. 19 shows the obtained values of X_I. Fig. 20 shows the obtained percentage values of the harmonics relative to the main harmonic from the 3rd till the 199st harmonic, and a 2% of the main harmonic.

The four H-bridges of the CMLI are switched so many times as for the single phase CMLI, shown in Fig. 12.

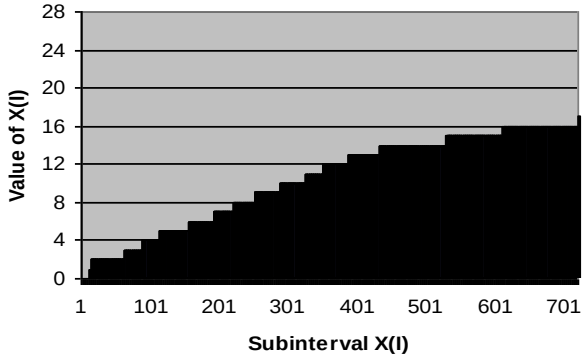

Fig15. *Values of X(I) that give V_1 = 16.22*

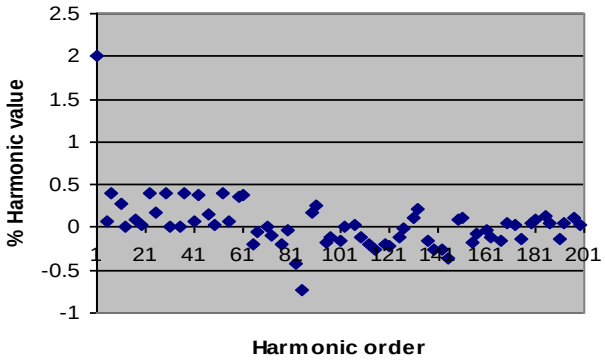

Fig16. *% Values of undesired harmonics for V_1 = 16.22*

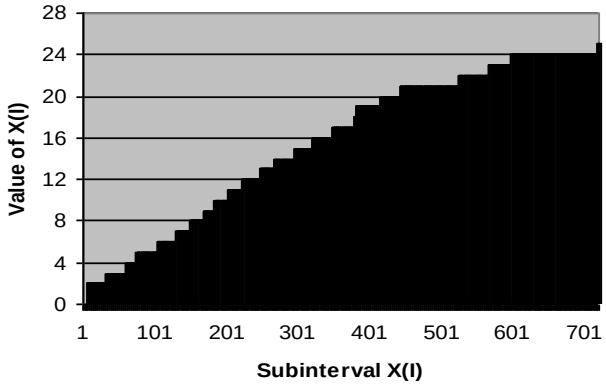

Fig17. *Values of X(I) that give V_1 = 24.26*

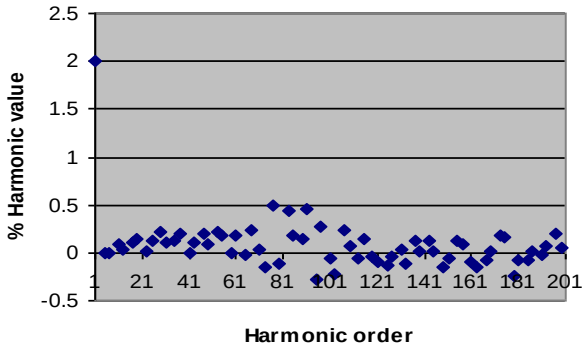

Fig18. *% Values of undesired harmonics for V_1 = 24.26*

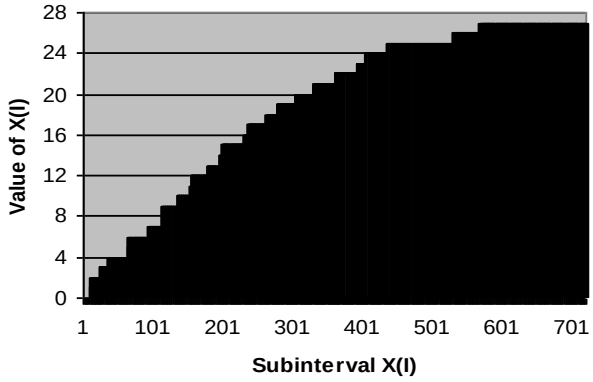

Fig19. *Values of X(I) that give V_1 = 2*

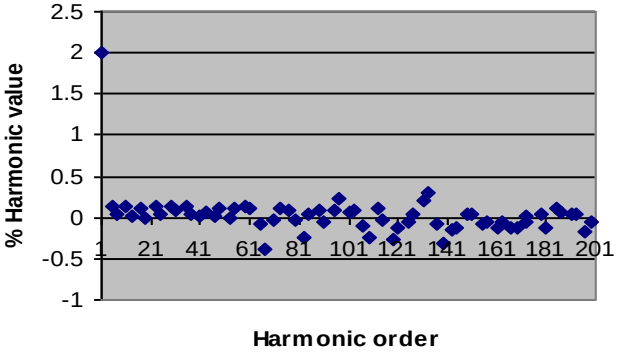

Fig20. *% Values of undesired harmonics for V1 = 29*

7. CONCLUSIONS

This paper introduces a general approach for minimizing the values of the undesired harmonics produced by symmetric or asymmetric uniform step CMLIs using a mixed integer linear programming (MILP) model, and applies it for single phase and three phase 55-level ACMLIs , with four H-bridges per phase. The H-bridges have dc sources E, 3E, 9E and 14E, for any arbitrarily chosen value of E. Using MILP for this problem has many advantages over other methods given in the literature, and specially of being suitable for ACMLIs with large number of levels. This approach is applied first to determine the number of harmonics to be minimized in order to obtain the least % THDE and % V_{LH} for an output voltage that is formed from all the 55 levels of the ACMLI. Then the result is used in the model when solving it for different values of the output voltage to obtain the switching pattern that minimize these harmonics values. Negligible values of % V_{LH} are obtained from these solutions. Solutions for single phase and three phase 55- level ACMLIs are given. For the single phase case it is noted that:

**The value of % V_{LH} is less than 1% for all output voltages between 14E and 28E, and less than 0.5% for all output voltages between 20E and 28E.

**The value of of % THDE is less than 5%, and the value of % V_{Hmax} is less than 3% for all output voltages between 14E and 29E, which agree with the IEEE standards 519-1992 for voltage distortion limits for output voltages ≤ 69kv., [14]

** The value of of % THDE is less than 2.5%, and the value of % V_{Hmax} is less than 1.5% for all output voltages between 20E and 28E, which agree with the IEEE standards 519-1992 for voltage distortion limits for output voltages between 69kv and 161kv, [14].

For the three phases case it is noted that:

**The value of % V_{LH} is less than 1% for all output voltages between 12E and 32E, and less than 0.5% for all output voltages between 18 and 30.

** The value of of % THDE is less than 2.5%, and the value of % V_{Hmax} is less than 1.5% for all output voltages between 16E and 32E, which agree with the IEEE standards 519-1992 for voltage distortion limits for output voltages between 69kv and 161kv., [14].

It should be noted that this proposed approach could be applied for symmetric or uniform step ACMLIs. The 55-level ACMLI needs only 4 series connected H-bridges per phase this will be at the cost of multiple switching losses, but this does not represent a serious problem with the recent development of power semiconductor switches with low switching losses.

In all the cases discussed the applied MILP model assumes dividing the quarter time cycle of the main harmonic in N=720 subintervals. This large value of N is chosen to get better results. The solution time on a usual personal computer for the most cases discussed in this paper takes very long time to obtain an exact optimum solution due to the large number (=N) of integer variables , which may exceed 2 hour, so near optimum solutions are mostly selected using a solution time limit of 1.5 hour. However, good solutions are obtained as shown above and in addition agree well with the IEEE standard 519-1992 for voltage distortion limits in power systems, [14]. This standard puts upper limits of 5 % and 3% for %THD and %V_{hmax} respectively for output voltages ≤ 69kv, and upper limits of 2.5 % and 1.5% for %THD and %V_{hmax} for output voltages between 69 and 161 kv. Thus using the results of this paper, the 55-level CMLI could be used for output voltage values till 161kv. for many single phase and three phase cases.

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AUTHOR'S BIOGRAPHY

M. EL-Bakry, was born in Cairo, Egypt on July 14, 1942. He obtained B.Sc. and M. Sc. degrees from the Faculty of Engineering of Cairo University 1963 and 1974 respectively, and Dr.-Ing. Degree from Bremen University, (W.) Germany 1979.

Since 1993 Dr. El-Bakry is working as professor of power electronics at the "Power Electronics and Energy Conversion Department" of the "Electronics Research Institute" in Dokki, Cairo, Egypt.

Dr. El-Bakry was nominated as "Consultant" in the field of "Electronic Control Systems in Industry" by the "Egyptian Engineering Syndicate, 1994. He shared in many practical projects, which are financed either nationally or internationally by the "USAIDS" and "NSF" of the USA.

Dr. El-Bakry published more than 70 papers in national and international journals and conferences, mainly in the fields of power electronics and energy conversion. He attended scientific meetings and conferences in many countries all over the world, including Australia, Belorussia, Canada, China, Egypt, Germany, Japan, Korea, Saudi Arabia, Syria, Turkey and USA.