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Design of IEEE 1394b Bus Link-layer Controller

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Abstract: *The IEEE 1394 bus has advantages such as high transmission speed, long transmission distance, plug and play, supporting variable transmission modes and so on. This essay mainly focuses on study link layer in the bus protocol and data transfer in asynchronous and isochronous mode, design the control chip for IEEE 1394b link layer, implements the design on RTL-level programming and verify the design through software simulation. Main work completed consists of: analyzes the protocol structure of link layer, physical layer of IEEE 1394b bus, defines the link layer control chip's function and system structure divided into modules. Implement the design of modules with RTL programming and simulates the design in software.*

Keywords: *IEEE 1394b, link layer, data transmission*

1. INTRODUCTION

Bus is a group of data cables transferring data and instructions between micro-processor and periphery devices and the core of interface part between those parts. IEEE 1394b bus is one of the main serial real-time bus standards with the advantages of high speed, long distance and plug-and-play and is widely used in connecting household computers and multimedia devices. Currently most IEEE 1394b bus communication control chip used inland are products from TI or VIA, and on the view of developing Chinese IC industry and national information safety, we should design and develop IEEE 1394 products with independent intellectual property rights.

2. OVERALL DESIGN OF IEEE 1394B BUS CONTROLLER

The IEEE134b agreement is shown in Fig.1. Based on the agreement, IEEE 1394b bus contains three layers: transaction layer, link layer and physical layer and services data transfer between data requester and data response. Each layer is relatively independent and connected through services.

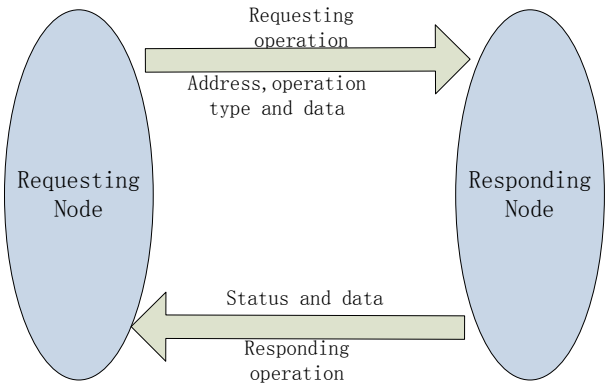

Figure1. *IEEE1394b bus agreement*

Link layer supports asynchronous and isochronous transfer, completes the addressing, data verifying and analysis for data packets. The link layer mainly services the transaction layer, turns transaction layer requests into corresponding packets and sub affairs to be transferred on bus later on.

IEEE 1394b bus link-layer controller (IP core) designed in this paper is to control the function of IEEE 1394b link-layer using FPGA instead of standard link-layer chip and realizes link-layer's role in transferring data.

The functions of link-layer controller are as follows: the link-layer core follows specifications in IEEE 1394b high-performance serial agreements and is able to transfer and receive IEEE 1394b data packet in both synchronous and isochronous mode; the physical layer interface is compatible with physical layer controller manufactured by TI and other physical layer devices in accordance with IEEE 1394b physical/link layer interface agreement. Supports data transfer at 100Mb/s, 200Mb/s, 400Mb/s and 800Mb/s and compatible with 1394 timing. Supports serial communication between 33Mhz/32bit(or 33Mhz/64 bit) local PCI bus and 1394b bus physical layer device.

The structure for 1394b bus link layer controller is as shown in Fig. 2, including nine modules: PCI host bus interface, Central Arbiter and PCI Initiator SM, Transmit FIFO, Receive FIFO, Transmitter, Receiver, Cycle Timer and Cycle Monitor, Internal Register and Physical Interface.

3. THE REALIZATION OF IEEE 1394B BUS CONTROLLER

3.1 PCI Host Bus Interface

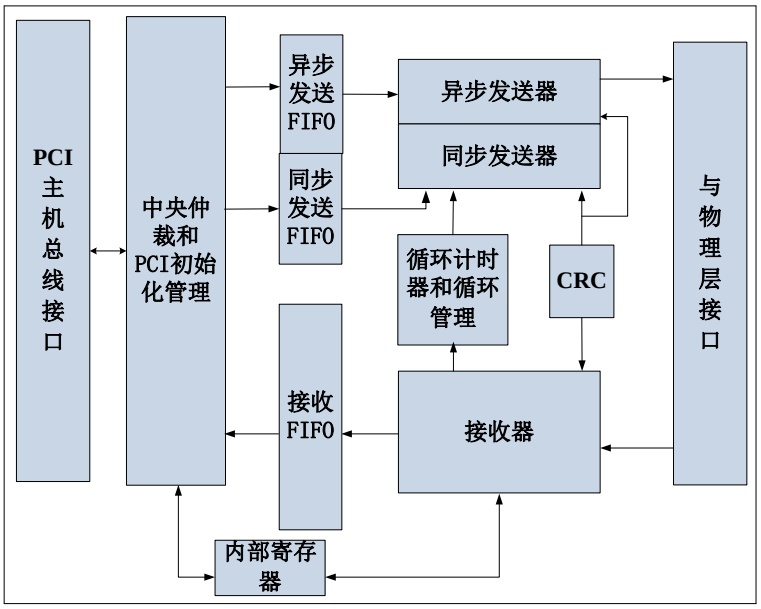

Figure 2. *1394b link layer controller structure*

The PCI host bus interface mainly implements the write of transaction layer information and read of link-layer control IP core information. The main duty is answer to host processor's bus period: at bus's write period, link-layer controller write bus data to FIFO or registers; at bus's read period, link layer controller read data to data bus from FIFO or registers, and give a CA# signal to end the bus period.

The link layer controller's answer to host's read period is shown in the left graph of Graph 3. At clock edge 1, CS# low effective is detected (a), while WR# is high effective (b), then data on the address bus is latched (c) into RD_ADDR(e), reading address of register, set signal RD_en high (d) and signal CA low (g) for one edge period at the clock edge . Register files or FIFO return RD_DATA based on address. When the RD_DATA is effective, the data would be sent to DATA(h). In design, CS# and WR# enables the register.

Link layer controller's respond to the host's read period is similar with its respond to the host's write period, the only different is that only address bus is latched and signal RD_en is set at clock edge 1.

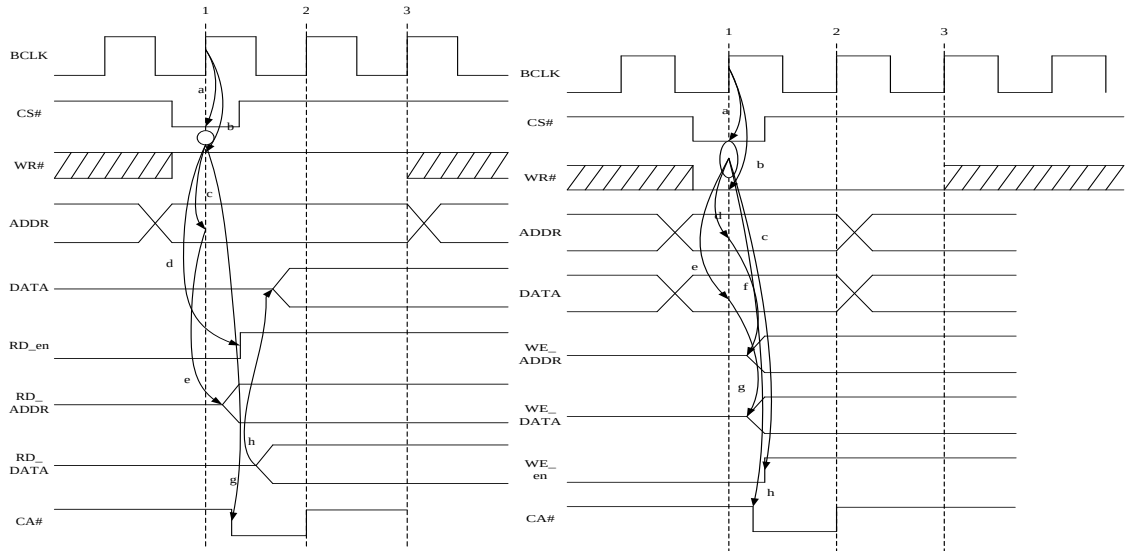

Figure 3. *Signal Respond during write period and read period*

Link layer controller's respond to Host's write period is shown in the right graph of Fig. 3. At clock edge 1, CS# and WR# is low effective (a,b), the data on address bus and data bus would be latched (d,e) to register's write address WE_ADDR and write data WE_DATA (f,g) , set signal WE_en high (c) and signal CA low for one edge period (h) at this clock edge. The three signals would be used by register files or FIFO based on address. In design, CS# and WR# enables the register.

3.2 FIFO

The main function is to cache data packets during sending and receiving those packets. Because the clock used by interfaces agreements between Transaction layer and link layer controller is different from the clock used by agreements between link layer controller and physical layer, so the timing sequences need a buffer between transmission and a FIFO is needed between two different clock domains.

1394b supports PCI burst transmission and depth FIFO used to permit large host delay. The FIFOs can be divided into 3 parts by functions: asynchronous transfer FIFO (AT FIFO for short) with 5K capacity; isochronous transfer FIFO(IT FIFO for short) with 2K capacity and general receive FIFO (GR FIFO for short) which are used for asynchronous transferring, isochronous transferring and data storage during transfer.

3.3 Transmitter

Transmitters include isochronous transmitters and asynchronous transmitters. The main job of asynchronous transmitters is to pack the data into a packet form appropriate for physical layer transfer and sent the packets to physical layer when the host write asynchronous data packet into AT FIFO. During the transfer, cycle redundancy check (CRC) is made to the packets and CRC code produced would be transferred when the data transfer is finished. The asynchronous transmitter has three functions: 1. The applying and releasing of serial bus; 2. The organization of head for asynchronous data packets; 3.Sending asynchronous data packets. The transmitter consists of 3 mainly modules based on the function: serial bus management module, packet head organization module and packet send module.

The main job of isochronous transmitters is pack data appropriate for PHY layer and send the data packets to PHY chip when Host CPU is about to write packets to send into IT FIFO, which is similar to the job of asynchronous transmitters. But there are also difference: during isochronous transfer, the packet head written by host is different from packet head to send, and the head needs to be re-organized. As for block data, the sending process is to read from IT FIFO and then send directly, adding CRC check at the end. The structure of asynchronous transmitter(left) and isochronous transmitter are shown in Fig. 4.

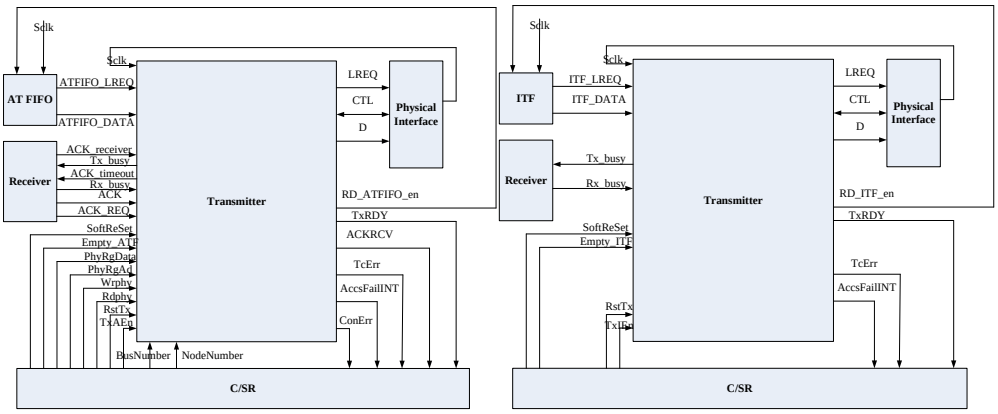

Figure 4. *The structure of asynchronous transmitter (left) and isochronous transmitter*

3.4 Receiver

Receiver receives the asynchronous or isochronous data packets sent by physical layer, transform the packet into appropriate form for transaction layer and store the data into GR FIFO. The transform is mainly focused on packet head while the block data in the packet can be stored directly into GR FIFO. As for asynchronous packets, CRC check is needed to make sure no mistake occurred during the transfer process.

4. TEST RESULT

Test is required when the design for IEEE 1394b bus link layer controller is finished. The test includes verifying the rightness for design and completeness for function. Here we use software simulation to verify the designed controller.

Software simulation includes 2 parts:(1)test for sub-modules;(2)test for overall code. The specific content is as follows:

The overall test for link layer controller: Organize all modules as one complete system, simulates host and physical layer to read data from or write data to the link layer controller.

Sending data: Simulates the write operation to link layer controller's host bus when the host is sending data, requires the controller to send bus request to physical layer through PHY interface and send data when bus authorization is obtained.

Receiving data: Simulates the communication between physical layer and link layer controller when receiving data. Requires the link layer controller to organize received data into GRF, send a interrupt request to the host. Then simulates host read operation to read data from link layer controller. The mainly simulation result is shown below (using ModelSim) in Fig. 5,6 and 7.

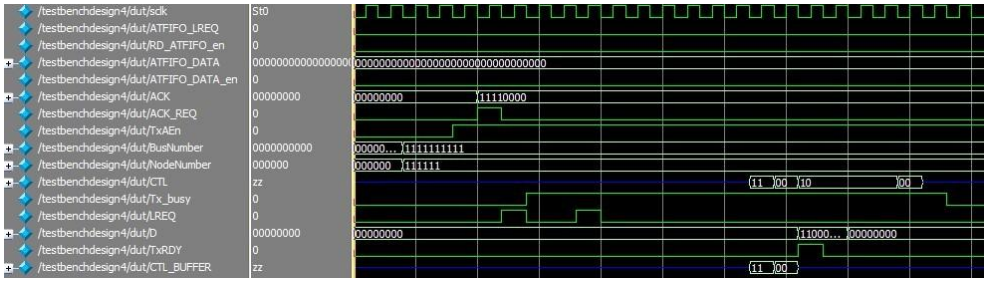

Figure 5. *asynchronous transmitter send data packets*

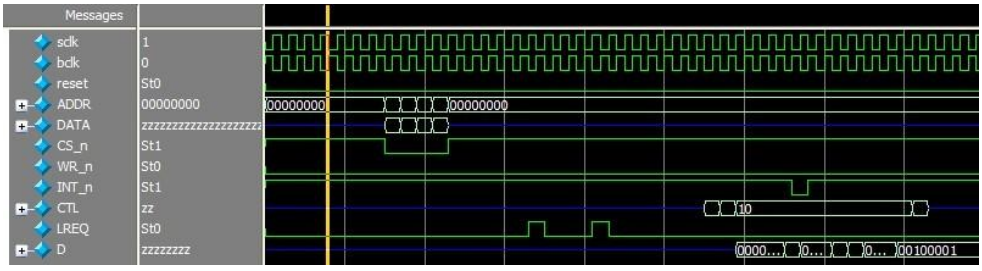

Figure 6. *Link layer controller send a 4-byte write request data packet*

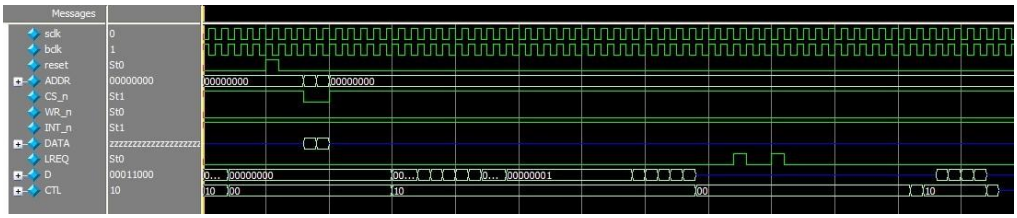

Figure 7. *Link layer receiving asynchronous data packets*

5. CONCLUSION

This paper analyzes the agreement structure of IEEE 1394b bus, pinpoints the function of link layer during data transfer. Based on asynchronous transfer model, isochronous transfer model and link layer function, defines the function and system structure model the controller should follows. Completes function-level design of link layer controller, actualizes the design in RTL level using hardware description language and simulates the design in software environment.

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