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A High Performance Flip-Flop Grouping Design with Integration of Clock Gating and Power Gating

Shaik Mohammed Rafi

M. Tech, Malla Reddy Engineering College (Autonomous), Hyderabad, India
mohammedrafi494@gmail.com

Chandragiri Bhanu Prakash

Associate Professor, Malla Reddy Engineering College (Autonomous), Hyderabad, India

Abstract: *In Integrated circuits a giant portion of chip power is spent by duration system that contains of temporal order components like flip-flops, latches and clock distribution network. This paper enumerates power economical style of shift registers mistreatment D flip-flops together with Clock and Power gating integration. Clock gating and power gating proves to be terribly effective solutions for reducing dynamic and active outpouring power severally. The 2 techniques square measure coupled in such the simplest way that the clock gating data is employed to drive the management signal of power-gating electronic equipment. During this paper, AN activity driven fine-grained clock and power gating is projected. First, a method named Optimized Bus-Specific-Clock-Gating (OBSC) is introduced that reduces the matter of gated flip-flop choice by applicable choice of set of flip-flops. Then another technique named Run Time Power Gating (RTPG) is projected for power gating the combinatory logics activity redundant operations. The projected shift registers square measure designed up to the layout level with 1V Power provide in zero.18um technology and simulated mistreatment Tanner Tools.*

Keywords: *Time Power Gating (RTPG), Optimized Bus-Specific-Clock-Gating (OBSC).*

1. INTRODUCTION

With the smaller geometries in Deep Sub-Micron (DSM) technology, the amount of gates that require to be integrated on one chip, power density, and total power are increasing speedily. Also, planning for low-power has become progressively necessary in a very large choice of applications. However, making optimum low-power styles involves trade like temporal order versus power and space versus power at the various stages of the look flow. Booming power-sensitive styles need engineers to own the power to accurately and expeditiously perform these trades.

To address these problems directly, it's essential to grasp the various sorts and sources of power dissipation in digital Complementary Metal chemical compound Semiconductor (CMOS) circuits. the rationale for selecting the CMOS technology is that it's presently the foremost dominant digital IC implementation technology. Power dissipation in CMOS digital circuits is categorized into 2 types: peak power and time-averaged power consumption. Peak power could be a reliableness issue that determines each the chip life and performance. The drop effects, caused by the excessive instant current owing through the resistive power network, affect the performance of a style as a result of the exaggerated gate and interconnect delay.

This massive power consumption causes the device to overheat that reduces the reliableness and lifelong of the circuit. Conjointly noise margins are reduced, increasing the possibility of chip failure

as a result of interference. A CMOS digital circuit happens in 2 forms: dynamic and static. Dynamic power dissipation happens within the logic gates that are within the method of change from one state to a different. Throughout this method, any internal and external capacitance related to the gate's transistors should be charged, thereby intense power. Static power dissipation is related to inactive logic gates (i.e., not presently change from one state to another). Dynamic power is very important throughout traditional operation, particularly at high operative frequencies, whereas static power is additional necessary throughout standby, particularly for powered devices.

For dynamic loss reduction we have a tendency to be victimization Clock Gating technique and for static loss reduction we have a tendency to are suing RTPG technique explained below.

2. CLOCK GATING AND POWER GATING

2.1. CLOCK GATING

Clock gating could be a well-liked technique utilized in several synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding additional logic to a circuit to prune the clock tree. Pruning the clock disables parts of the electronic equipment in order that the flip-flops in them don't have to be compelled to switch states. A change state consumes power. Once not being switched, the change power consumption goes to zero, and solely outflow currents are incurred. [1]

Clock gating works by taking the alter conditions connected to registers, and uses them to gate the clocks. Thus it's imperative that a style should contain these alter conditions so as to use and like clock gating.

This clock gating method may also save vital die space similarly as power, since it removes massive numbers of muxe's and replaces them with clock gating logic. This clock gating logic is mostly within the variety of "Integrated clock gating" (ICG) cells. However, note that the clock gating logic can amendment the clock tree structure, since the clock gating logic can sit within the clock tree.

2.2. POWER GATING

Could be a technique utilized in microcircuit style to scale back power consumption, by motion off this to blocks of the circuit that aren't in use. Additionally to reducing stand-by or outflow power, power gating has the advantage of sanctioning Iddq testing.

3. PROBLEM STATEMENT

This analysis work is titled new low power approaches for VLSI logic and memory. whereas planning a VLSI system power dissipation is one amongst the foremost considerations. Up to a precise time dynamic power was the one largest concern; but because the technology feature size shrinks static power has become a very important issue as dynamic power.

Clock Gating (CG) is that the commonest and wide used technique to scale back dynamic power, and Power Gating (PG) is that the dominant technique to scale back standby outflow power. As active outflow power becomes additional and additional necessary, it conjointly needs care. so as to differentiate it from the standard PG, that is employed to scale back the standby outflow, the PG to attenuate active outflow power within the operation mode is mentioned as Run Time Power Gating (RTPG). CG could be a technique accustomed gate the excess clock toggles of a register. throughout the clock gated amount, there are some elements that are performing arts redundant operations, and RTPG can place these elements into sleep.

There are many researchers that specialize in the mixing of CG and RTPG. All of their styles ar supported clock gated styles generated when synthesis and those they assess the practicability of

RTPG per the signal activity of the look. However, it's attainable that a style cannot be clock gated throughout synthesis. Then their approach cannot be used. Moreover, with the signal activity of the look, CG ought to even be analyzed to see if dynamic power is reduced. If dynamic power is exaggerated, the entire power could increase even though active outflow power is reduced.

We have projected Associate in nursing activity-driven fine-grained CG and RTPG integration, which may scale back dynamic power and active outflow power at the same time. Associate in nursing activity-driven Optimized Bus Specific Clock Gating (OBSC afterward) is employed to maximize dynamic power reduction at resistance junction transistor (RT) level before synthesis. It chooses solely a set of Flip-Flops (FF) to be gated by selection, and therefore the drawback of gated FF choice is reduced from exponential quality into linear. When the OBSC is applied to the look, the elements performing arts redundant operations throughout the clock gated amount are determined by forward traversing the circuit from the gated FF outputs. These elements are going to be power gated victimization the clock alter signal generated by OBSC providing the implementation of RTPG will scale back active outflow power.

We have projected a fine-grained CG Associate in Nursingd RTPG integration supported signal activities with an activity driven fine-grained OBSC technique that selects solely a set of FFs to gate. It will scale back dynamic power by victimization the latch based mostly AND Clock Gating and reduces the outflow power by employing a sleep junction transistor. Moreover, the clock alter signal generated within the OBSC circuit is used because the sleep signal in RTPG. The ability gated cells is determined by forward traversing from the gated FF outputs. Each Clock Gating and Power Gating ways are wonderful during this regard.

Our goal is to trade off between these limitations and therefore propose new ways that scale back each outflow and dynamic power with minimum attainable space and delay trade off.

Here we classified the shift register to three places

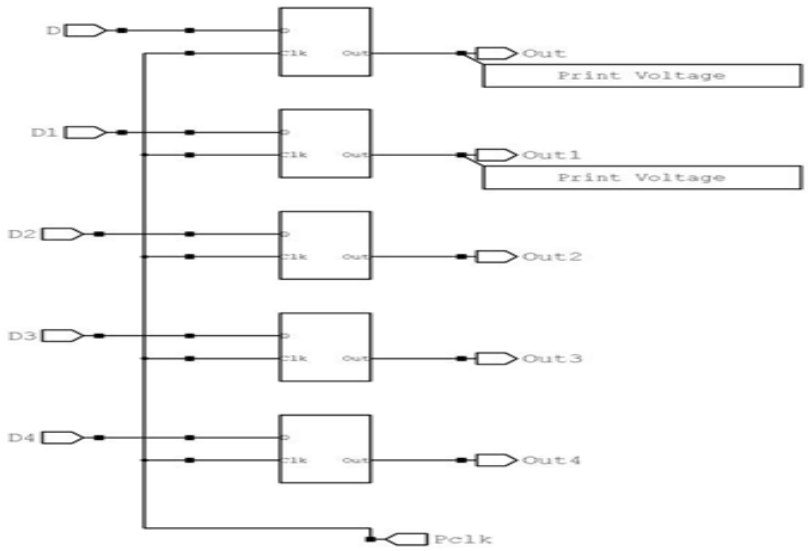

Fig1. *Non Clock Gating Circuit*

4. PROPOSED OBSC

Optimized Bus Specific Clock Gating is extremely effective technique to maximize dynamic power reduction as shown in fig.5. It chooses solely a set of flip-flops (FF) to be gated by selection, and therefore the drawback of gated FF choice is reduced from exponential complexness into linear. It works by comparison the inputs and outputs and gates the clock once they area unit equal [11].

Considering N FFs within the non-CG circuit, every FF may be chosen as gated or non-gated. Hence, 2N CG solutions area unit potential and therefore the exponential complexness drawback is reduced into linear. Assume that each one the FFs area unit chosen to be gated at first, and so the matter is in decisive that FFs ought to be excluded from gating [1]. Heuristically, the FF with the most output knowledge toggle rate ought to be excluded from gating 1st.

This is as a result of that most output knowledge toggle rate indicates that minimum clock toggles are gated, so power can cut back least or maybe increase if the FF is gated. a lot of formally, the FF with the most output toggle rate is excluded from gating 1st, then the FF with the second largest output toggle rate is excluded then on till all the FFs area unit excluded (i.e., the initial non CG circuit). Apparently, throughout the method of exclusion, there'll be N+1 potential CG solutions

This is linear complexity.

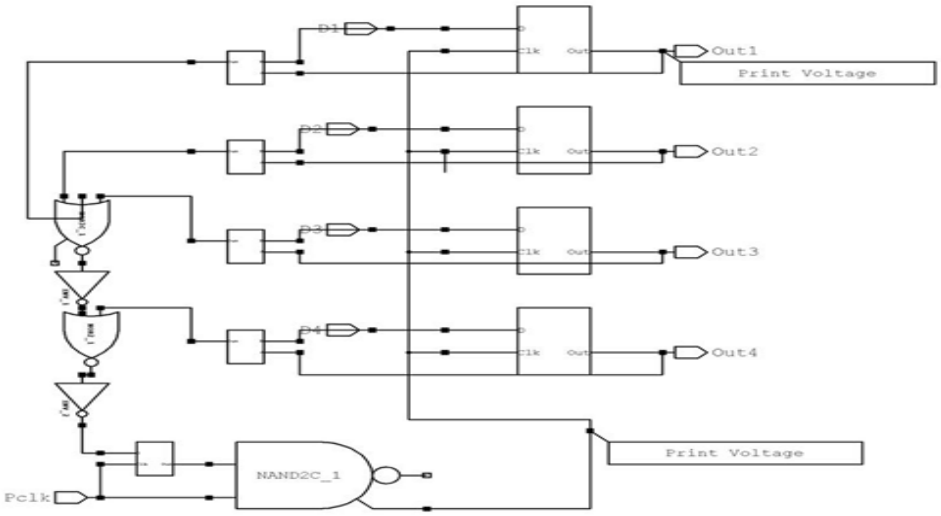

Fig2. *PBSC circuit*

In order to realize integration of CG and RTPG, apply OBSC technique to the planning, then a set of FFs is clock gated. Throughout the clock gated amount, the outputs of the gated FFs square measure stable.

Consequently, those combinatory logics whose inputs solely depend upon gated FF outputs are going to be inactive and might be power gated as shown in Fig half-dozen. For every output of the ability gated cell, whether or not a affiliation to primary output presence needs to be checked. Holder logic ought to be added so as to avoid signal floating. Suppose that four out of 5 FFs square measure clock gated. The circled cells square measure utterly smitten by the stable gated FF outputs, so that they don't seem to be active and might be power gated into sleep [1]. However, one input of the XOR gate i is that the output of un-gated FF A, and one input of the AND circuit h is that the primary input. Since each the un-gated FF output and PI might not be stable throughout the clock gated amount, the XOR gate i and also the AND h could also be active. So that they mustn't be power gated. In order to avoid floating signal, a holder ought to be placed at the output of every power gated cell if that output connects to non power gated cells or primary outputs (Pos)

If RTPG needs to be applied, footer (high-Vth CMOS transistor) between the particular ground and virtual ground of the ability gated cells ought to be added. Once the combination of CG and RTPG, the low power style ought to seem like Fig.6.The modify signal generated from OBSC is employed because the sleep signal for the PG. The cells that square measure completely smitten by gated FF

outputs square measure power gated. Holder's square measure placed between the ability gated cells and also the non power gated cells so the non power gated cells will operate properly.

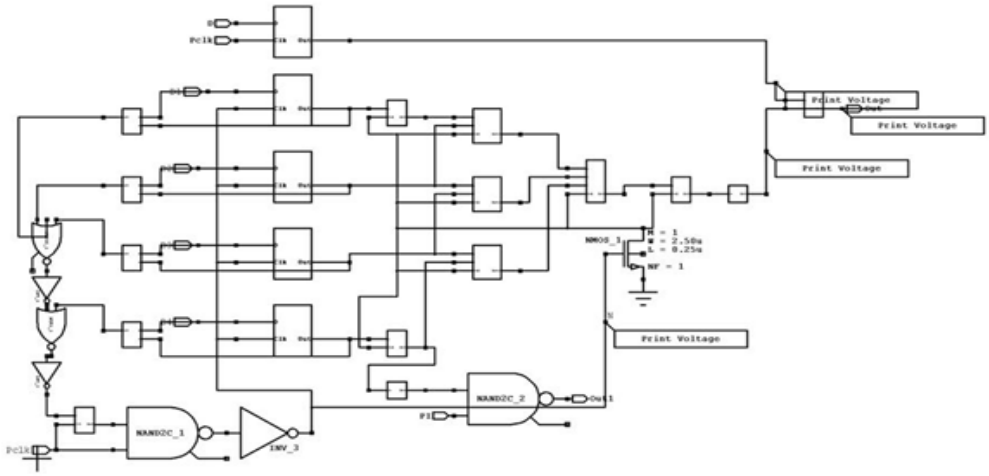

Fig3. *Integration of OBSC and RTPG*

If RTPG has to be applied, footer (high-Vth CMOS transistor) between the actual ground and virtual ground of the power gated cells should be added. After the integration of CG and RTPG, the low power design should look like Fig.6.The enable signal generated from OBSC is used as the sleep signal for the PG. The cells that are totally dependent on gated FF outputs are power gated. Holders are placed between the power gated cells and the non power gated cells so that the non power gated cells can function properly.

5. VARIABLE BODY BIASING TECHNIQUE

This is another new leakage reduction technique, which we call the ''Variable body biasing'' technique.

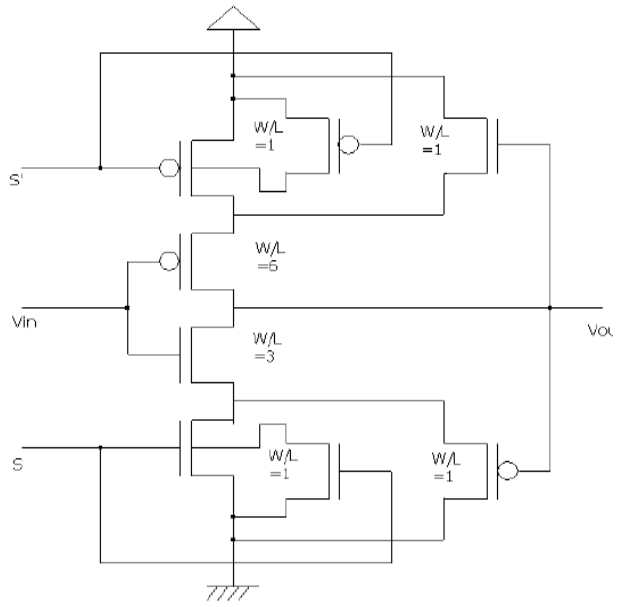

Fig4. *Structure of variable body biasing technique with sleep method*

This technique in figure uses 2 parallel connected sleep transistors in Vdd and 2 parallel connected sleep transistors in GND. The supply of 1 of the pmos sleep semiconductor device electronic

transistor semiconductor device semiconductor unit semiconductor} is connected to the body of alternative pmos sleep transistor for having therefore known as body biasing impact. Equally the supply of 1 of the nmos sleep semiconductor device electronic transistor semiconductor device semiconductor unit semiconductor} is connected to the body of alternative nmos sleep transistor for having constant impact as for pmos sleep transistors. So, escape reduction during this technique happens in 2 ways in which. Firstly, the sleep semiconductor unit impact and second, the variable body biasing impact. it's documented that pmos transistors aren't economical at passing GND; equally, it's documented that nmos transistors aren't economical at passing Vdd. however this variable body biasing technique uses pmos semiconductor device electronic transistor|semiconductor device|semiconductor unit|semiconductor} in GND and nmos transistor in Vdd, each square measure in paralleled to the sleep transistors, for maintaining actual logic state throughout sleep mode. this system uses ratio W/L=3 for nmos semiconductor device|electronic transistor|semiconductor device|semiconductor unit|semiconductor} and W/L=6 for pmos transistor within the main electrical converter portion. For the sleep transistors this system uses ratio W/L=1 for each the nmos and pmos transistors. the additional 2 transistors of the planning for maintaining the logic state throughout sleep mode conjointly use ratio W/L=1. Thanks to the minimum ratio the sub-threshold current reduces.

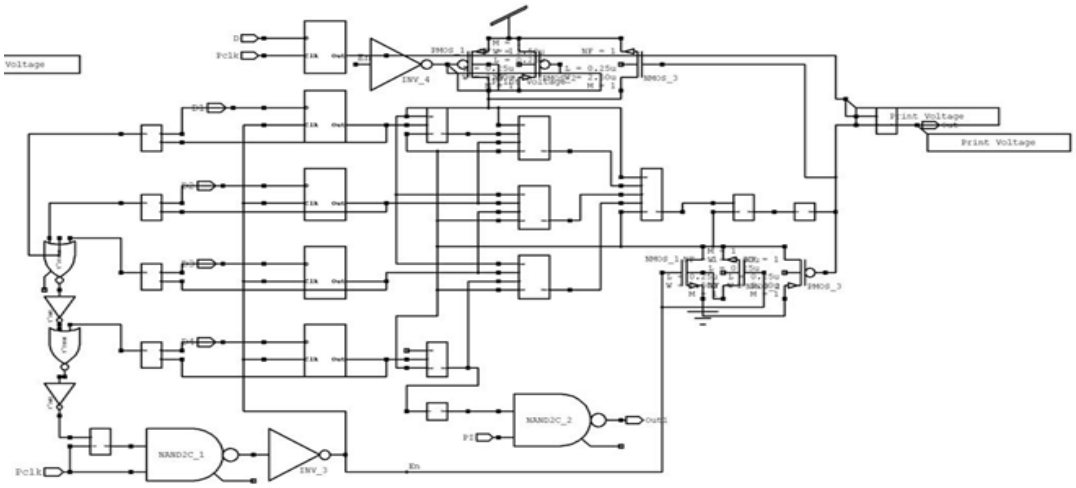

Fig5. *Integration of OBSC and RTPG with Variable Body-bias Technique*

Circuit	Power Dissipation
Integration of OBSC and RTPG with sleep	4.113243 e^{-002} W
Integration of OBSC and RTPG with Variable body bias technique	5.995837 e^{-003} W

6. CONCLUSION

In this Paper, a fine-grained CG and RTPG integration is achieved in ordered circuits. First, AN activity driven fine-grained OBSC technique is evaluated that selects solely a set of FFs to gate. Moreover, the clock alter signal generated within the OBSC circuit is used because the sleep signal in RTPG. Following this, ordered circuits that implements each OBSC and RTPG is taken into account and their performances are evaluated with sleep and variable body bias technique mistreatment Tanner Tools.

7. FUTURE SCOPE

For Integration of clock gating we have a tendency to should check concerning the delay created the clock gating network thus in future we will style which might cut back the delay created by the clock gating electronic equipment.

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AUTHOR'S BIOGRAPHY

Shaik Mohammed Rafi, Currently Studying M.Tech: Vlsi System Design At Malla Reddy Engineering College (Autonomous), Hyderabad, India. B.Tech. Nimra College of Engineering and Technology, Affiliated To Jntu Kakinada (2008-2012), Vijayawada**.** Field of Interest: Vlsi Design, Communication.

Chandragiri Bhanu Prakash, Currently Working As an Associate Professor in Malla Reddy Engineering College (Autonomous), Hyderabad, India. M.Tech: Vasavi College of Engineering, Hyderabad (2009). B.Tech: Mgit, Gandipet, Hyderabad (2006). Experience: 7 Years Teaching. Field of Interest: Communication, Vlsi Design.