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Effect of Number of Subcarriers on Implementation of OFDM Transceiver on FPGA

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Abstract: *Orthogonal Frequency Division Multiplexing (OFDM) is a communication system where multiple carriers are used to transmit the data. It is popularly used because of it is very much robust to frequency selective distorted channels. In this paper, we are focusing on the design and an implementation of OFDM transceiver on FPGA. VHDL is used in implementation of the system, high level synthesis tool is used for synthesis and it is targeted on Xilinx Spartan 3e device. ISE simulator is used to simulate presented design and the results are presented. This paper presents resources utilization for transmitter and receiver when 4 and 8 subcarriers are used. For floating point multiplication, addition subtraction and division required for design we are utilizing the Intellectual Property (IP) cores provided by Xilinx. To calculate IFFT and FFT we are using DIT radix-2 butterfly approach.*

Keywords: *FPGA, FFT, IFFT, DIT, ISE, VHDL.*

1. INTRODUCTION

Baseband OFDM for multi-carrier transceiver is increasingly being used by the modern digital mobile communication systems. OFDM is having high spectral efficiency because it uses the idea of elimination of guard bands and use of the overlapping but orthogonal subcarriers. We are dividing high rate data stream is into a number of low rate data streams that are transmitted over a number of multiplexed orthogonal subcarriers [1]. The low rate data streams allow us to add sufficient guard time between two symbols which was very small in high rate data stream. This helps us in enabling the system to perform well in dispersive channel which causes the symbols to spread in time and interfere with each other this phenomenon is called as 'Inter symbol interference (ISI)**'.** OFDM can be viewed as combination of a modulation and multiplexing technique, and its hierarchy lies in the physical and medium access layer. A basic OFDM transceiver consists of a QAM or PSK modulator/demodulator (depending on spectral efficiency), a serial to parallel/parallel to serial converter, and an IFFT/FFT module [1]. The block diagram of basic OFDM system is shown in Fig 1. The transmitter has an input bit stream, serial to parallel converter, constellation mapping, IFFT, Digital to Analog Converter. The receiver has an Analog to Digital Converter, FFT, parallel to serial converter, demodulation, and output bit stream. Organization of this paper is as follows. In Section II we are presenting the design flow of implementation of an OFDM transceiver from system design to circuitry realization on FPGA. The detailed demonstration of implementation of the transmitter and receiver are demonstrated in section III and IV. We are presenting the results in section V and finally we are concluding the paper in section VI.

2. DESIGN FLOW

Implementation of transmitter and receiver is done independently and tested it on FPGA, and then both the subsystems were merged to form one system. We designed the system for two sets of subcarriers one is using 4 subcarriers and the other using 8 subcarriers. Design flow for both the system is same. It is explained as follows. Before designing the system we started with the understanding of the block diagram. It gave the idea about operations which are needed to be performed on FPGA. Then we developed the algorithm for sequential and concurrent operations. To make the design more parallel, the operations are broken in to processes and independently written in VHDL. Some blocks need floating point complex operations, for that Intellectual

Property (IP) cores provided by Xilinx, are used. All types of floating operations are done on IP cores. The system is designed completely on Xilinx Project Navigator using VHDL coding as design entry method. Then the system is simulated on ISE simulator for timing analysis. Finally the design is synthesized on FPGA Spartan 3e device using high level synthesis tool.

2.1 Transmitter Design

2.1.1 Transmitter Design Flow

16 bit long input data stream is stored in an array using VHDL. Simultaneously, serial to parallel conversion is done in independent process along with mapping of the parallel, grouped bits in to complex constellation for QPSK. Real and imaginary parts of constellation points are stored two different arrays. Look up table is utilized for mapping of grouped bits in to constellation points. Complex multiplications are needed to be performed for 8 point IFFT calculations. Twiddle factors are stored in array, which are necessarily floating point. An algorithm is developed for the floating point complex multiplications. IFFT processor is multistate process which uses different IP cores for predefined operations. Two separate systems are designed using 4 subcarriers and 8 subcarriers. To have different number of subcarriers means changing the number of points in IFFT processor. A separate process maps the real and imaginary values in the range of DAC and transmits them through separate channels. DAC used for this purpose is LTC 2624 which is interfaced with FPGA through SPI communication. For transmitting particular OFDM symbol through DAC it must be converted in the format that is acceptable by DAC. Then this control word is transmitted serially to DAC with control signals to start the conversion.

2.1.2 Comparative Analysis of Transmitters

4 subcarriers and 8 subcarriers are used to implement presented system. The effect on computational complexity to calculate the IFFT of increasing the number of subcarriers is shown in Table I. Number of clock cycles required to perform the operation are given in Table I.

Number of operations required on a one set of data to convert it from bit stream to OFDM symbol is described in Table I. The comparison shows that 8 point system requires more time but it receives more number of bits per OFDM symbol, it means its spectral efficiency is more.

2.2 Receiver Design

Receiver is designed on the same board for presented system. After the IFFT block the data is directly given to FFT block in receiver. The design flow of the receiver and the comparison between 4 point and 8 point receiver is presented in following sections.

2.2.1 Receiver Design Flow

Design of receiver is done separately before connecting it to transmitter. FFT is calculated using same algorithm which is developed for transmitter. DIT radix-2 butterfly is used to calculate FFT and IFFT. Xilinx Project Navigator and VHDL coding is used to design the receiver. Similar to transmitter, floating point complex multiplication, additions and subtractions in receiver are done using the IP cores. Operations of receiver are broken in to different processes and merged to have complete system. After FFT operation, demodulation is done by using look up table approach. The reception is completed once the bits are recovered from the received constellation. Separate receivers are designed and tested for 4 points and 8 points transmitter. ISE simulator is used once the design code is ready for timing analysis and then code is synthesized on kit.

2.2.2 Comparative Analysis of Receiver

For 4 point transmitter and 8 point transmitter receivers are different. In this section the different receivers are compared on the basis of computational complexity and time in terms of number of clock cycles required to perform the operation. The comparison is shown in Table I.

Table I describes the number of operations required to be done on each data set to convert it from bit stream to OFDM symbol. The comparison shows that more time is required for 8 point system than 4 point system but it receives more number of bits per OFDM symbol. Both the transmitter and receiver are simulated on ISE before they are synthesizing them on FPGA.

ISE results help in understanding the timing ambiguities and in resolving the conflicts between different internal signals. Results of simulation is compared in Table II in next section and based on that the conclusion can be made.

3. FIGURES AND TABLES

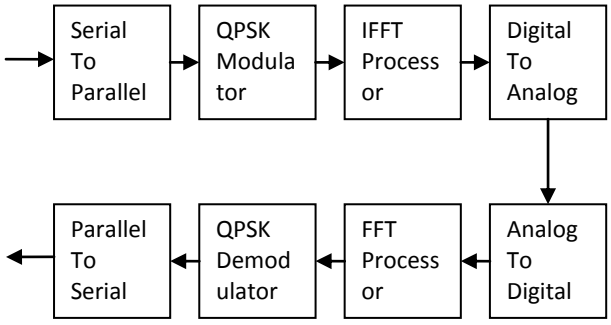

Fig 1. *Block diagram of basic baseband OFDM system*

Table I. *comparative analysis of transmitters and receivers*

Parameter	Transmitter		Receiver	
	4 point	**8 point**	**4 point**	**8 point**
Number of Complex multiplications	1	5	1	5
Number of Complex additions	8	24	8	24
Number of divisions	8	16	8	16
Number of clocks for multiplications	1	95	1	95
Number of clocks for additions	2	75	2	75
Number of bits in an OFDM symbol	8	16	8	16

Table III. *comparative analysis of transmitters and receivers for device utilization*

Logic Utilization	Transmitter			Receiver		
	used	**present**	**Usage**	**used**	**present**	**Usage**
Number of Slice Flip Flops	3195	9312	34%	3228	9312	34%
Number of 4 input LUTs	7828	9312	84%	5366	9312	57%
Number of occupied slices	4448	4656	95%	4032	4656	86%
Number of slices containing related logic	4448	4448	100%	4032	4032	100%
Number of slices containing unrelated logic	0	4448	0%	0	4448	0%
Total Number of 4 input LUTs	7924	9312	85%	5437	9312	58%
Number of bonded IOBs	74	232	31%	4	232	1%
Number of MULT 18X18 SIOs	4	20	2%	4	20	2%

4. CONCLUSION

Goal of this paper is hardware implementation of OFDM system on Spartan 3 FPGA using VHDL language for designing the system. The system design procedure, tools and results are discussed in this paper. Conclusion that can be made from the results of simulation is, processing time required to calculate IFFT and FFT increases as there is increase in the number of subcarriers in the system,. Spectral efficiency of the system is increased as number of subcarriers is the increased.

Results show that the system is working properly. Device utilization of the transmitter and receiver shows that the device is utilized well bellow its maximum. Further by increasing the number of subcarriers and by making highly pipelined architecture for IFFT and FFT the system performance could be improved in terms of processing time required in transmitter and receiver.

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